Observation on Wall Charge Leakage During Address Period Under Variable Panel Temperature

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ABSTRACT

To explain the address discharge fail at a high temperature, the wall charge leakage phenomenon during an address-period was investigated relative to the number of applied address and sustain pulses under variable panel temperatures based on the V_t closed-curve analysis. The wall charge leakages were increased with an increase in the number of the applied address and sustain pulse, and this tendency are intensified as the panel temperature increased. The wall voltage leakage causes a weakening of the address discharge, thereby resulting in increase in the address delay. Furthermore, the effects of ITO width on the wall charge leakage during an address-period were also examined under variable panel temperatures. It was observed that the wall voltage leakages were increased with an increase in the ITO width.

1. INTRODUCTION

Recently, the image qualities of plasma display panels have grown rapidly and considerably [1]. However, the further improvement of an image quality in AC-PDPs, especially full high definition (HD) PDP requires wider driving margin and more stable discharge. The panel temperature or ambient temperature is one of the important factors for producing the stable discharge in the PDP cells because the discharge characteristics are varied depending on the panel temperature. Nonetheless, the intense research on the relation between the panel temperature and the discharge characteristics has often been neglected [2, 3].

In this paper, to explain the address discharge fail at a high temperature, the wall charge leakage phenomenon during an address period was investigated relative to the number of applied address and sustain pulses under variable panel temperatures based on the V_t closed-curve analysis. Furthermore, the effects of ITO width on the wall charge leakage during an address period were also examined under variable panel temperatures.

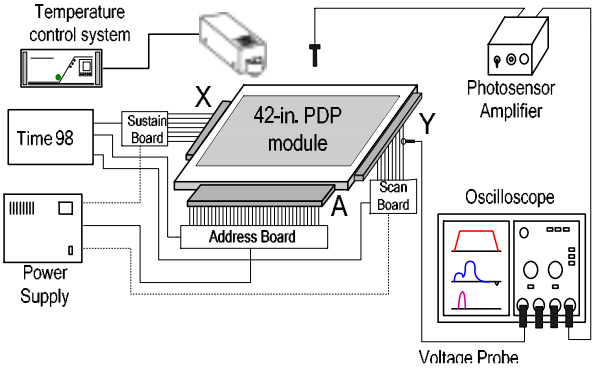


Fig. 1 Schematic diagram of experimental setup employed in this work

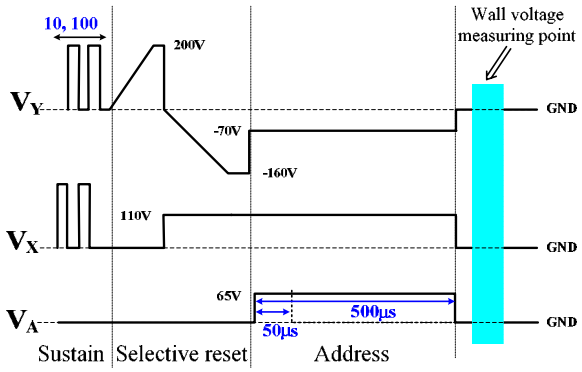
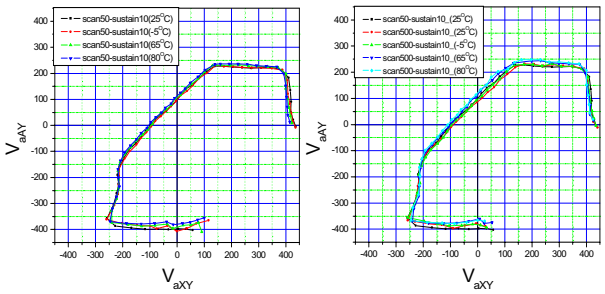


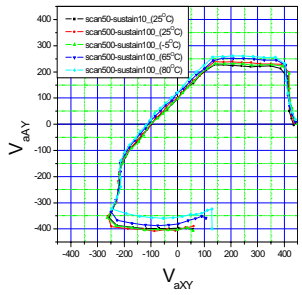
Fig. 2 Driving waveform employed for measuring wall charge leakages during address-period.

2. OBSERVAION ON WALL CHARGE LEAKAGE DURING ADDRESS PERIOD UNDER VARIABLE PANEL TEMPERATURE

Fig.1 shows the schematic diagram of the experimental setup for measurement. The 42-in. panel with a gas mixture of Ne-He-Xe (11 %) and a pressure of 450 Torr was employed in this research, and its structure and dimensions were the same as the conventional 42-in. wide XGA grade PDP. The panel temperature was varied from –5 to 80 ^{o}C by partially heating the glass with an external heater. Fig. 2 shows the driving waveform employed to measure the wall



(a) Scan50-Sustain10 (b) Scan500-Sustain10



(c) Scan500-Sustain100

Fig. 3 Measured Vt close curve relative to the number of applied address pulse and sustain pulse under variable panel temperature.

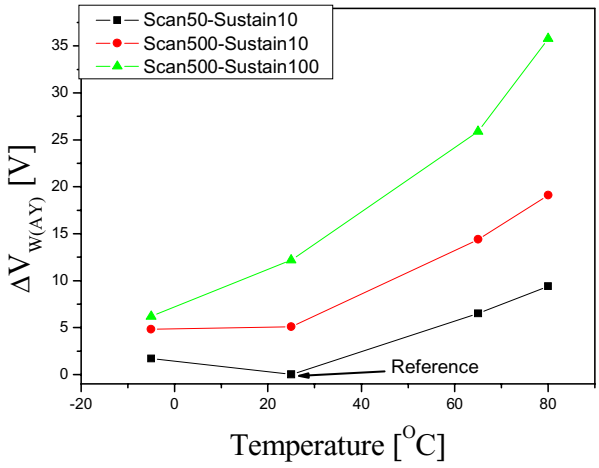


Fig. 4 Variation of wall voltage between A and Y electrode according to panel temperature

charge leakage during an address period. The applied sustain pulses were 10 pairs for the lower sub-field (SF3) and 100 pairs for the upper sub-field (SF10). In addition, the conditions for address pulses are given as follows: an address pulse width of 1.25 μs, that is, the address periods were 50 μs for 40 scan lines and 500 μs for 400 scan lines.

Fig. 3 shows the V_t closed-curves measured from the 42-in. panel relative to the number of the applied address sustain pulses under variable panel temperature. As the panel temperature was increased, the V_t close-curve was moved to upward direction, that is, the direction to reduce the wall voltage between the A-

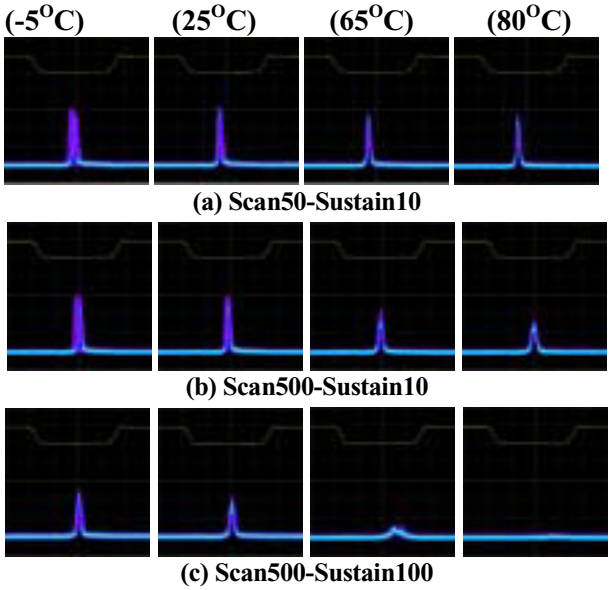


Fig. 5 IR intensities emitted during an address discharge relative to the number of applied address pulse and sustain pulse under variable panel temperature.

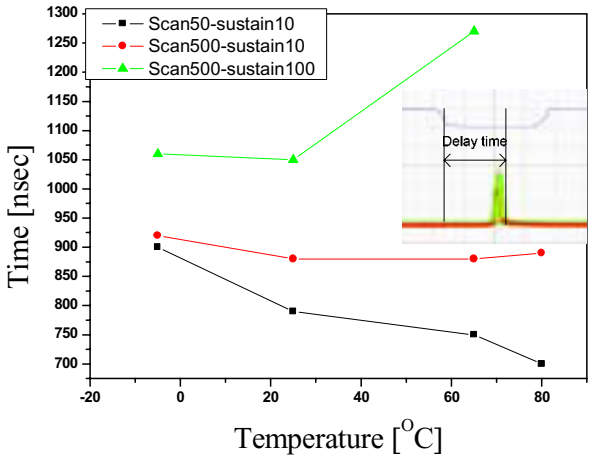
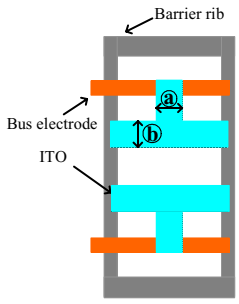


Fig. 6 Variations in address discharge delay relative to panel temperature

Y electrodes. The wall voltage reduction between the A-Y electrodes was larger with an increase in the number of address and sustains pulses.

Fig. 4 shows the variations in the wall voltage between the A-Y electrodes relative to the number of applied address and sustain pulses under variable panel temperature. The wall charge leakage was increased at higher panel temperature, which would be caused by the change of MgO surface resistivity with the panel temperature [4]. The corresponding IR intensities emitted during an address discharge were measured, as shown Fig. 5. As the panel temperature was increased, the IR intensity was decreased. The IR intensities were also diminished in proportion to the increase in the number of address and sustain pulses. Fig. 6 shows the



	ⓐ	ⓑ
Case Ⅰ	150㎛	50㎛
Case Ⅱ	50㎛	50㎛
Case Ⅲ	150㎛	90㎛
Case Ⅳ	100㎛	50㎛
Case Ⅴ	100㎛	90㎛
Case Ⅵ	100㎛	70㎛

Fig. 7 Cell structure and condition of ITO width used in this experiment

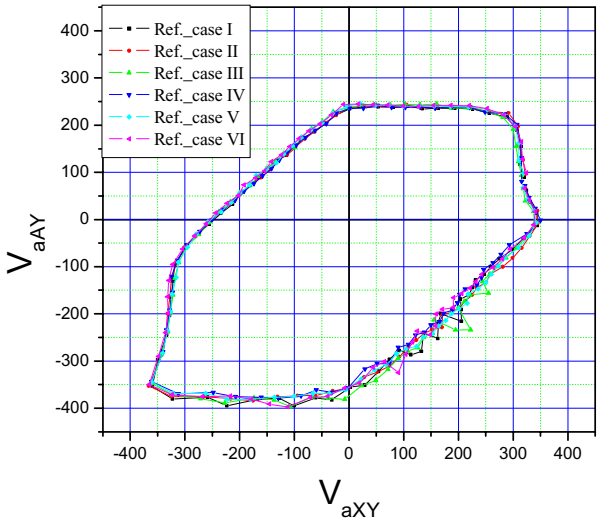


Fig. 8 The measured Vt close curve of various ITO width in zero wall voltage condition at room temperature

variations in the address delay time relative to the panel temperature at different sustain and address pulse numbers. For the 500 μs-scan and 100-sustain pulse condition, the address delay time was increased at the higher panel temperature, which would be caused by the wall charge leakage during an address-period at a higher temperature. However, for the 50 μs-scan and 10- sustain pulse condition, the address delay time was decreased at a higher temperature. This improvement of address discharge delay at higher temperature is due to the small wall voltage variation between the A-Y electrode at higher temperature, and also due to the facilitation of the address discharge caused by the change in the partial gas density at higher temperature [5].

3. EFFECT OF ITO WIDTH ON WALL CHARGE LEAKAGE DURING ADDRESS PERIOD UNDER VARIABLE PANEL TEMPERATURE

Fig. 7 shows the cell structure of T-shape electrode with different ITO widths used in this experiment. When the ITO width (ⓐ and ⓑ) was varied from case

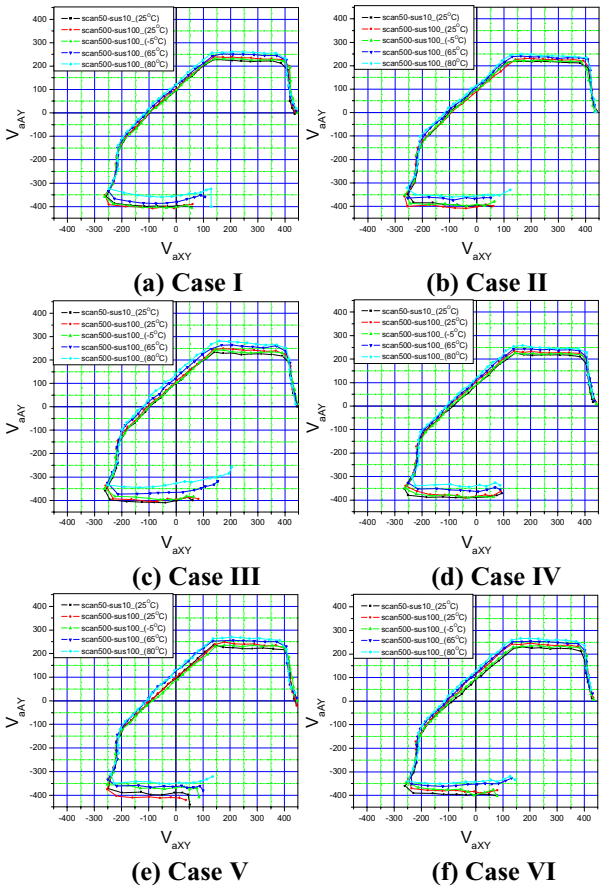


Fig. 9 Vt closed-curves measured from 42-in. panel of variable ITO width condition

Table. 1. Firing voltages between A-Y electrodes obtained from Vt closed-curves in Fig. 9

	Scan50-Sustain10 (25°C)	Scan500-Sustain100			
		-5 °C	25 °C	65 °C	80 °C
Case I	222.1V	228.3V	234.3V	248V	257.9V
Case II	216.2V	220.4V	226.3V	235.5V	242.6V
Case III	226.2V	235.3V	243.1V	259.7V	272.2V
Case IV	217.5V	222.3V	228.5V	240.4V	249.4V
Case V	223.7V	232.2V	239.5V	252.6V	263.9V
Case VI	223.4V	231.2V	239.3V	250V	260.9V

Ⅰ to case Ⅵ, as shown Fig. 7, the wall charge leakage during an address period and related address discharge characteristics were investigated. Fig. 8 shows the measured V_t closed-curve with no initial wall charge relative to the ITO width. The firing voltages were observed to be almost the same irrespective of the ITO width.

Fig. 9 shows the V_t closed-curves from the 42-in. panel relative to the ITO width at different panel temperatures and applied address and sustain pulses. From the measured V_t close-curves shown in Fig. 9, the firing voltage between the A-Y electrodes are given in Table1.

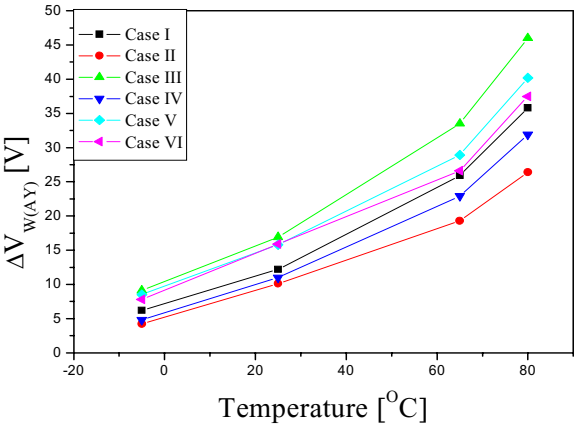


Fig. 10 Variation of wall voltage under variable panel temperature relative to change of ITO width

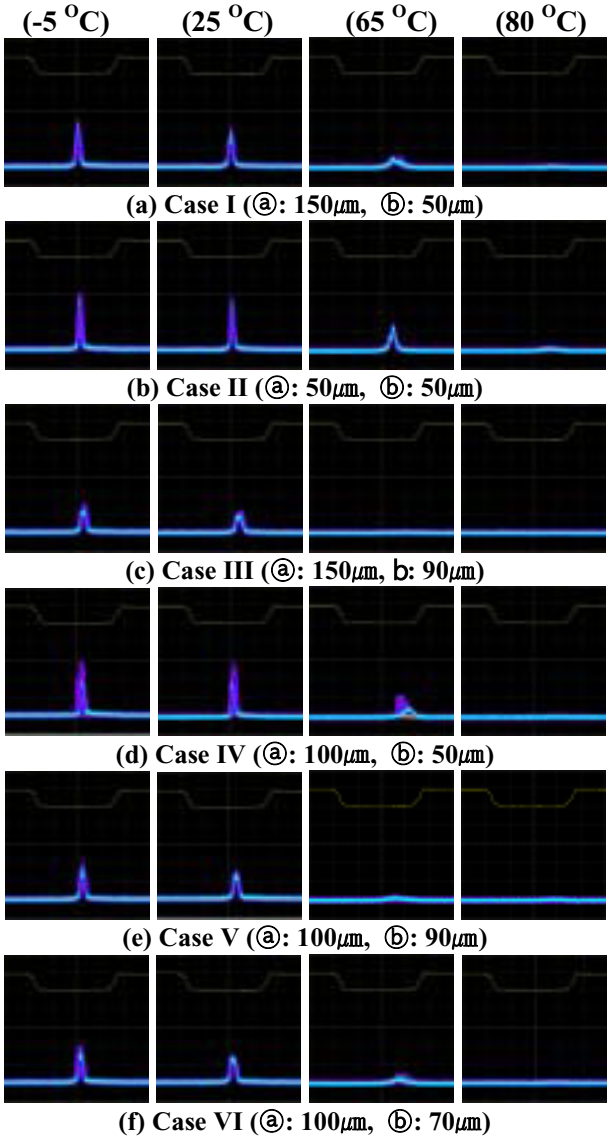


Fig. 10 Variation of IR intensity during address discharge under variable panel temperature according to change of ITO width

Fig. 10 shows the variations in the wall voltage under variable panel temperature relative to the ITO width. As the panel temperature was increased, the wall voltage variation between the A-Y electrodes was increased. For case Ⅲ, the wall charge change was shown to be maximal, whereas for case Ⅱ, the wall charge change was shown to be minimal. The wall charge leakage was increased in proportion to the ITO width. Fig. 11 shows the variations in the IR intensity during an address discharge under variable panel temperature relative to the ITO width. As the ITO width was increased, the variation in the IR emission was also increased.

4. CONCLUSION

In view of discharge instability, the relation between the discharge characteristics and the panel temperature is very important. This paper describes the wall charge leakage phenomenon during an address-period relative to the number of applied address and sustain pulses under variable panel temperature base on the Vt closed-curve analysis. In addition, the effects of the ITO width on the wall charge leakage were also examined in detail.

6. REFERENCES

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