New Reset While Address (RWA) Driving Scheme for Single Scan of XGA Grade AC PDP with High Xe Content

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ABSTRACT

A new reset-while-address (RWA) driving scheme for a single scan of XGA grade (1024 x 768) AC PDP is proposed to improve the address discharge characteristics under high Xe gas mixture (15 %). In order to solve the conventional address problem such as the gradual decrease of the priming particles during an address-period, the falling ramp-waveform in the reset-period is separated into the two parts; the one part of the falling ramp-waveform applied in the reset-period provides the priming particles during the first half address-period, and the other part of the falling ramp-waveform applied in the middle of the address-period provides the priming particles once more during the second half address-period. As a result of adopting the proposed RWA driving scheme, the address discharges were produced within 1.0 μs pulse width successfully thanks to the presence of the priming particles throughout the address-period.

INTRODUCTION

The cost of a current PDP-TVs should be lowered below the reasonable price urgently to preoccupy a TV consumer market [1]. The dual scan driving method for XGA grade PDPs that uses the two pairs of address driver IC for addressing the two part of the screen, is one of the high price factors of a PDP-TV, when compared with a single scan method. In the current technology, however, it is difficult to display the full high definition panel by means of the single scan method [2]. This difficulty is caused by the weak discharge or discharge-fail due to the lack of priming particles, especially after the first half address-period. Moreover, the production of the address discharge would be more difficult under high Xe gas mixture condition without priming particles [3]. It has been reported that the address discharge characteristics can be improved by producing the priming particles from adjacent cells [4] or by increasing the address voltage gradually from the first to the last address pulse [5]. However, the use of the priming particles causes not only a misfiring discharge but also an increase in the background light. The gradual increase in the address voltage causes a complex address circuit as well as a high cost of the address driving circuit.

In this work, a new reset-while-address (RWA) driving scheme is proposed for supplying priming particles once more during address-period without any side effect in 42-inch XGA grade PDP with 15 % Xe gas mixture. In the case of adopting the proposed driving scheme, the address discharge time lags was examined and compared with those in the case of adopting the conventional driving scheme.

CONVENTIONAL DRIVING WAVEFORM

Fig. 1 shows the conventional driving waveforms for 42-inch XGA grade PDP with 15% Xe gas mixture, which include the reset-, address-, and sustain-periods. The distribution of priming particles during an address-period is also shown in the lower part of Fig. 1. Since the large amount of priming particles are produced when applying the falling ramp waveform during a reset-period, the density of priming particles in a cell decreases gradually as the line-by-line address procedure is carried out. When applying the address pulse with

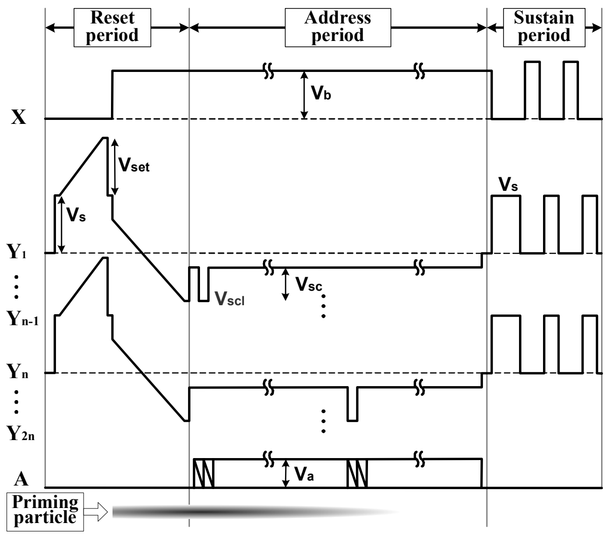
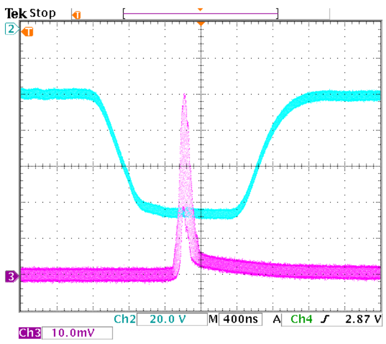


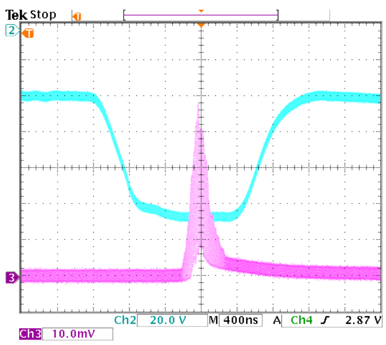
Fig. 1. Conventional driving waveforms and priming particles distribution during an address-period.

amplitude of 70V and width of 1.5 µs, the Light waveforms measured during an address-period at the first, middle and, last scan times are shown in Fig. 2. As shown in Fig. 2, under many priming particles during a first half address-period, the address discharge time lags are short and its intensity is strong, whereas under less priming particles during a second half address-period, the address discharge time lags are long and its intensity is weak. Fig. 3 illustrates the changes in the address discharge time lags at the first, middle, and last scan times when applying the conventional driving waveforms shown in Fig. 1. When the scan time was changed from the first to the middle scan time, the formative time lags increases slightly but the statistical time lags increases much.

(a)



(b)



(c)

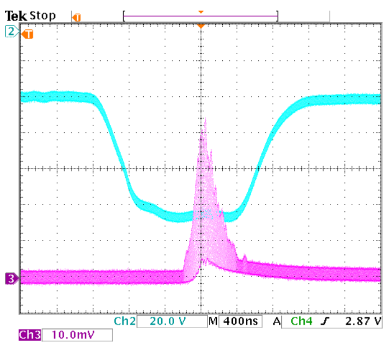


Fig. 2. Scan voltage and light waveforms measured during address-period at (a) first, (b) middle, and (c) last scan time, when applying conventional driving waveform with address voltage of 70 V and scan pulse width of 1.5 µs.

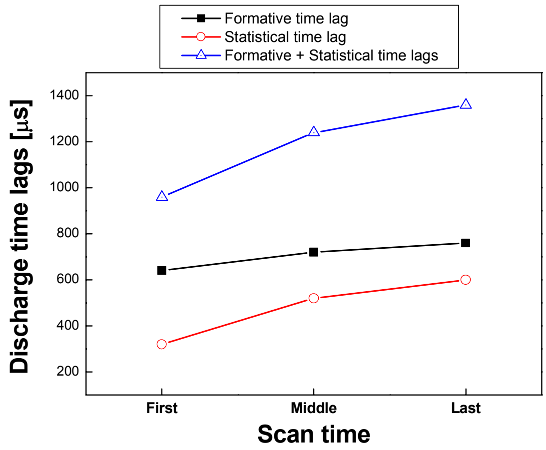


Fig. 3 Changes in discharge time lags at first, middle, and last scan time in case of adopting conventional driving waveform.

That means that the priming particles disappear almost after the middle scan time because it takes a long time from the generation of priming particles during the reset-period. The reduction of the priming particles during an address-period causes the increase in the address voltage and address discharge failure.

NEW DRIVING WAVEFORM

The different address voltage margins are induced depending on the difference in the scan time in the conventional driving scheme. In particular, to improve the address discharge characteristics with high Xe content during from the middle to the last scan time, the priming particles needs to be supplied in the middle of an address-period. In this sense, the new driving waveform for the RWA scheme, which can supply the priming particles once more in the middle of the address-period, was designed, as shown in Fig. 4. The falling ramp waveform for producing the priming particles was separated into the two parts: the first falling ramp in the reset 1 period plays a role in supplying the priming particles during a first half address-period from the first to the n^{th} scan line and the second falling ramp in the reset 2 period plays a role in providing the priming particles during a second half address-period from the $n+1^{th}$.to the $2n^{th}$ scan line. In this scheme, the scan voltage, $V_{sc}(=V_{sch}-V_{scl})$, *i.e.,* the voltage difference between the scan high voltage (V_{sch}) and the scan low voltage (V_{scl}) remained constant in order not to raise the cost of the driving circuit.

In the proposed RWA scheme, the common bias voltage, V_x applied to the sustain X electrode can be adjusted during the first and second half address-period on condition that the misfiring discharge can be prevented between the sustain X and scan Y electrodes.

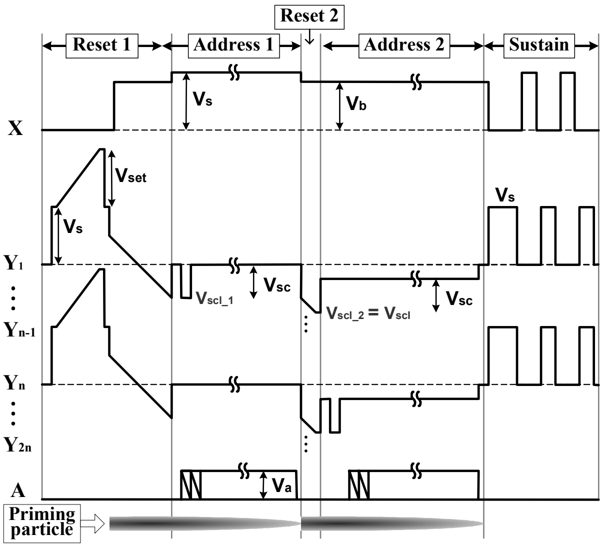


Fig. 4. RWA driving scheme with two groups and priming particle distribution during address -period.

In the proposed RWA driving scheme, since the lots of priming particles exist during a first half address-period, the scan-low voltage level, V_{scl_1} was increased to the low negative voltage level when compared with the conventional scan-low voltage (V_{scl}). The resultant common bias voltage, Vx was also increased slightly during the first half address-period so as to compensate a weak address discharge caused by the small potential difference between the scan Y and address A electrodes. The higher common bias voltage, V_x ($>V_b$) during the first half address-period induced the more wall charge accumulation at the initiation of the address discharge because the voltage difference between the sustain X and scan Y electrodes was large. In the reset 2 period of the proposed RWA driving scheme, the low scan voltage level (V_{scl_2}) should be lower than that in the reset 1 period so as to produce the priming particles once more, which means that the reset and sustain voltage levels of the proposed waveform were the same as those of the conventional waveform.

Fig. 5 shows the light waveforms measured during address-period at the (a) first, (b) middle, and (c) last scan time, in the case of applying the RWA driving waveform with an address voltage of 70 V and scan pulse width of 1.0 μs. It was observed that in the RWA driving scheme, the discharge time lags were shortened and the intensities of the IR emission were improved, especially in the middle and last case, when compared with the conventional address discharge shown in Fig. 2. Fig. 6 illustrates the changes in the address discharge time lags at the first, middle, and last scan times when applying the RWA driving waveforms shown in Fig. 4.

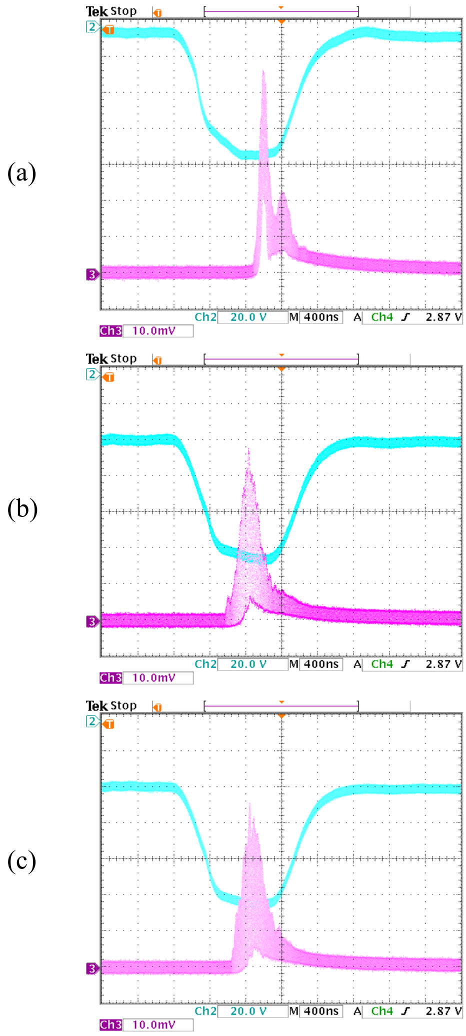


Fig. 5. Scan voltage and light waveforms measured during address-period at (a) first, (b) middle, and (c) last scan time, in case of applying RWA driving waveform with address voltage of 70 V and scan pulse width of 1.0 μs.

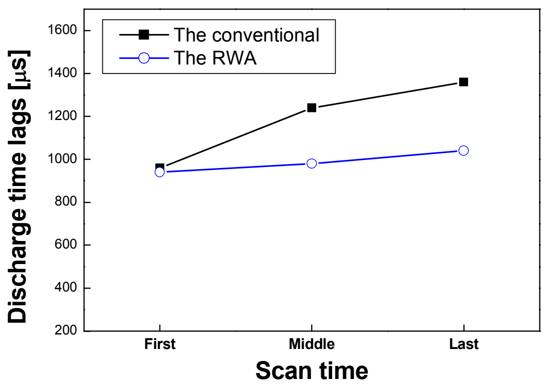


Fig. 6 Changes in discharge time lags at first, middle, and last scan time in case of adopting RWA driving waveform.

	Conventional	RWA
Minimum address voltage [V]	72	63
Background Luminance [cd/m^2]	0.12	0.12

Table. 1 Comparison of minimum address voltage and background luminance when adopting conventional and RWA driving schemes.

The address discharge time lags were much increased with an increase in the scan time in the conventional case, but for the proposed RWA driving scheme, the address discharge time lags were increased slightly, as shown in Fig. 6. The difference in the address discharge time lags between the conventional and RWA driving schemes was about 300 ns at the last scan time. The priming particles supplied by the falling reset ramp during the reset 2 period contribute to improving the address discharge characteristics under the high Xe gas environment after the first half address-period.

The minimum address voltage and background luminance were measured and compared in the Table 1 when applying the conventional and RWA driving waveforms. The result of Table 1 shows that the proposed RWA driving scheme can reduce the minimum address voltage by about 9 V in the scan pulse width of 1.0 μs condition under the almost same background luminance as the conventional case.

CONCLUSION

This work focuses on the design and examination of the new reset-while-address (RWA) driving scheme for improving the address discharge characteristics under high Xe gas mixture (15 %) so as to solve the conventional address problem such as the gradual decrease in the priming particles during an address-period. When compared with the conventional driving waveform, the RWA driving scheme shown in case of Fig. 4 can successfully produce the address discharge within 1.0 μs pulse width in the XGA grade PDP with high Xe (15 %) content thanks to the presence of the priming particles throughout the address-period.

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