New Multi-Level Scan Method for Improving Address Discharge Characteristics in AC PDP

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ABSTRACT

A new multi-level scan driving method with different scan low voltages under the same ramp falling voltage is proposed to improve the address discharge characteristics in the subsidiary subfields. When adopting the single-level scan method with the same scan low voltage, the address discharge time lag in the subsidiary subfield is lengthened over 200 ns compared with the first subfield using the main ramp reset waveform. By adopting the multi-level scan method, it is found that the address discharge in the second subfield can be reduced as much as that in the first subfield.

INTRODUCTION

Plasma display panels (PDPs) have been one of the most promising large areas over 40 inch flat panel device suitable for digital televisions. To compete the other displays in a large size area, however, the cost reduction of the driving circuits in the present AC PDP with three electrodes must be realized. One of the best cost reduction methods is to shorten the address time for single scan driving and lower the address voltage, thereby considerably lowering the cost of the address circuit. An Address Display-period Separation (ADS) driving scheme has been considered to be the most stable driving method in the current AC PDP [1]. However, the long address time during an address period in the ADS driving scheme is still a critical issue to be solved for the high quality AC PDP. For the realization of a high definition (HD) PDP with a large area greater than 40 inch and low power consumption by address pulses, an address pulse width should be shortened below 1 μs under the low address voltage condition [2]. The long address time is fundamentally due to the formative and statistical time lag phenomena in the address discharge [3, 4].

The amount of the wall charges accumulated between the scan (Y) and address (A) electrodes during a reset period determines the width and amplitude of the address pulse. However, the conventional reset waveform can not accumulate a sufficient amount of the wall charges between the scan (Y) and address (A) electrodes because the considerable amount of the wall charges are removed during a falling ramp period in order to make a zero wall voltage between the sustain (X) and scan (Y) electrodes for preventing a misfiring discharge. In this study, the reset waveforms are designed to minimize the loss of the wall charges accumulated between the Y and A electrodes prior to an address discharge. In this paper, a new driving method of reducing the address discharge time lag is introduced by using the V_t close-curve analysis during the first subfield adopting the main reset waveform. In addition, new multi-level scan method during an address periods is suggested to improve the address discharge characteristic after the disappearance of the priming particles during subsidiary subfields.

ADDRESS DISCHARGE CHARACTERISTICS

Fig. 1 shows the driving waveform with various voltages of ΔV_y (=V_{nf} - V_{scl}). In conventional case, a part of the wall charges accumulated on the Y and A electrodes during a falling ramp period are eliminated due to the gap voltage difference between the external and wall voltages during a falling ramp period. As the address discharge intensity is proportional to the external address voltage plus the wall voltage, a high address voltage should be applied to compensate the loss of wall charges. On the other hand, in this case, the negative falling voltage (V_{nf}) is higher than the scan low voltage (V_{scl}) in order to minimize the elimination of the wall charges that has already been accumulated on the Y and A electrodes during the rising ramp period compared with the same voltage between V_{nf} and V_{scl}. As the voltage of ΔV_y increases at the constant voltage

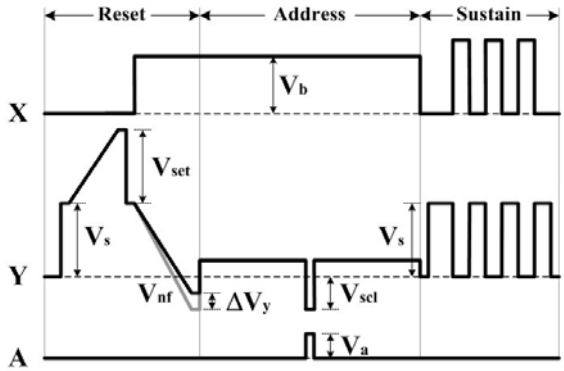


Fig. 1. Driving waveform with various ΔV_y ($V_{nf} - V_{scl}$).

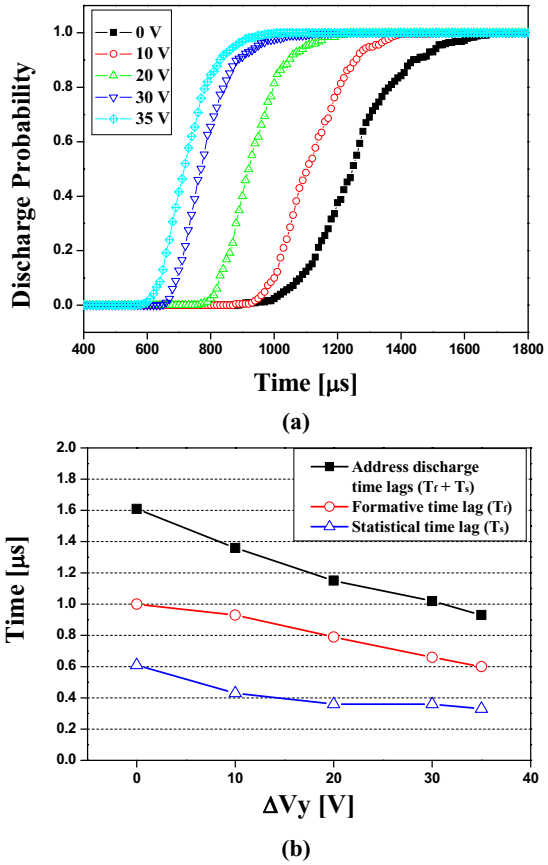


Fig. 2. (a) Address discharge probability with respect to time after applying scan pulse to PDP cell and (b) changes in address discharge time lags with various ΔV_y.

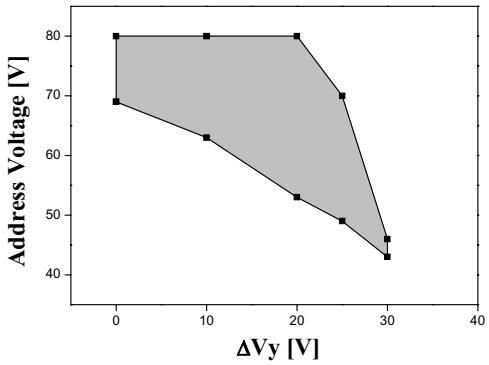


Fig. 3. Address voltage margin with increase in ΔV_y when applying the driving waveform of Fig. 1.

of V_{scl}, the loss of the wall charges during the falling ramp period is minimized, thus resulting in contributing the reduction of the address discharge time lag.

Fig. 2 shows (a) the address discharge probabilities of a PDP cells after applying the scan pulse and (b) changes in address discharge time lags when ΔV_y is 0, 10, 20, 30, and 35 V with a V_{scl} of -70 V. In case of the ΔV_y over 30 V, the address discharge time lag is shortened below scan pulse width of sub microsecond. Fig. 3 shows the address voltage margin with an increase in ΔV_y when applying the driving waveform

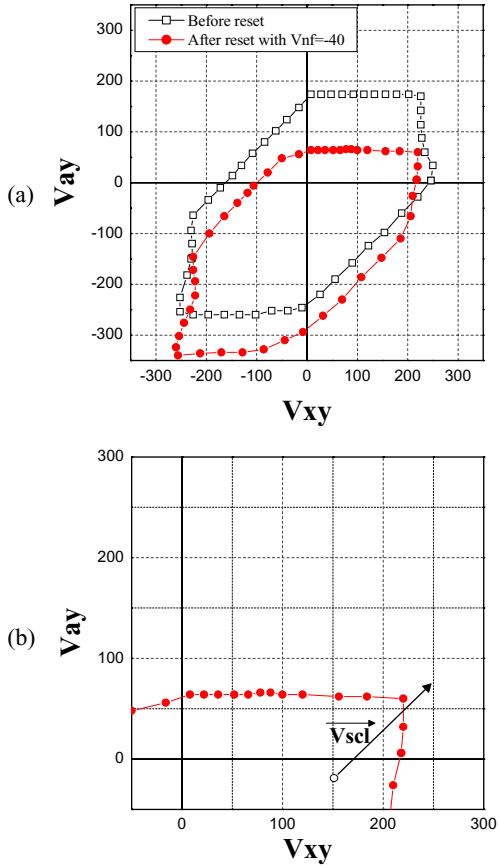


Fig. 4. (a) V_t close-curves on applied voltage plane measured from 42-in. PDP before and after applying a reset waveform with V_{nf} = -40 V and (b) enlarged V_t close-curve on first side measured after reset period.

of Fig. 1 with an address pulse width of 1 μs. As shown in the voltage margin data of Fig. 3, the maximum voltage was decreased over ΔV_y of 20 V due to the misfiring discharge. That means the value of ΔV_y has a limitation.

Fig. 4 (a) shows the two different V_t close-curves on the applied voltage plane measured before and after the reset period when applying the conventional driving waveform with 30 V of ΔV_y on Y electrode in Fig. 1. The six sides of the V_t close-curve in Fig. 4 (a) mean the threshold voltages, and the inner region of the V_t close-curve in Fig. 4 (a) means a non-discharge region, while the outer region means a discharge region. As shown by the V_t close-curves in Fig. 4 (a) measured before and after the reset period, the discharge start threshold cell voltage between the X (or Y) and Y (or X) electrodes, V_{tXY} (or V_{tYX}) is not changed, whereas the discharge start threshold cell voltage between the A (or Y) and Y (or A) electrodes, V_{tAY} (or V_{tYA}) is changed. Therefore, the V_t close-curves in Fig. 4 (a) illustrate that the changes in the accumulating wall charges occurred predominantly between the Y and A electrodes through the reset discharge, thus resulting in changes in the threshold voltage between the Y and A

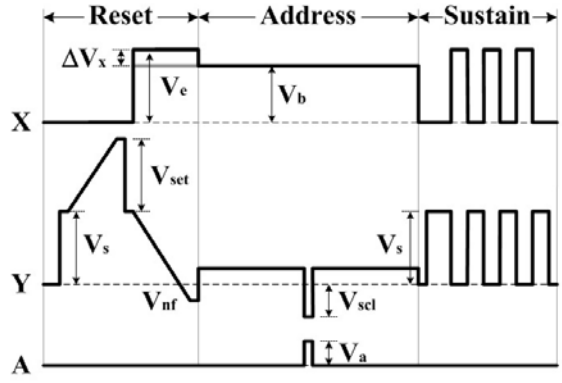


Fig. 5. Proposed driving waveform with V_e voltage for preventing misfiring discharge between X and Y electrodes.

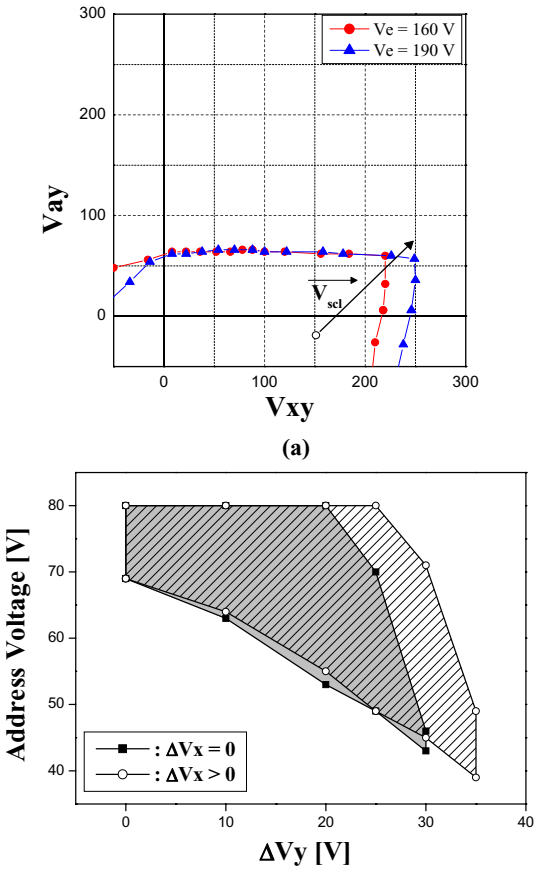


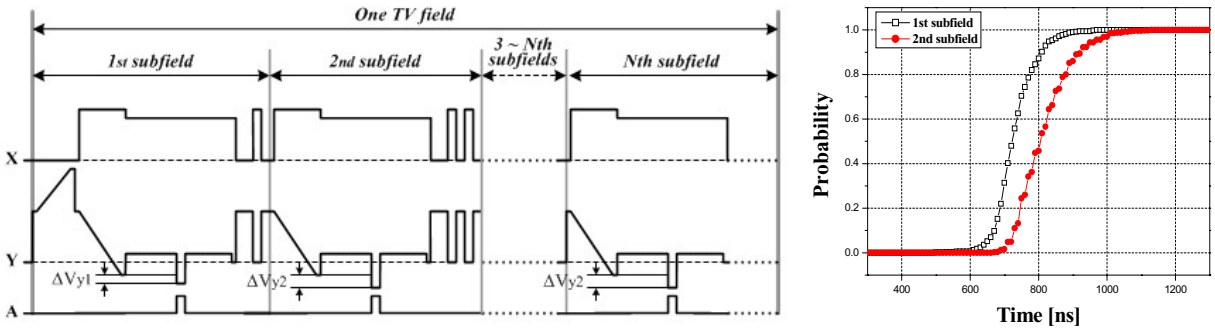
Fig. 6. (a) Enlarged V_t close-curve on first side of applied voltage plane measured after reset period and (b) changes in address voltage margin with increase in ΔV_y (b) when ΔV_x = 0 V (V_e = 160 V) and ΔV_x = 30 V (V_e = 190 V).

electrodes. The horizontal axis for the cell voltage plane in Fig. 4 (a) represents the potential difference, V_{xy} (=V_x - V_y) between the X and Y electrodes, whereas the vertical axis represents the potential difference, V_{ay} (=V_a - V_y) between the A and Y electrodes. Fig. 4 (b) shows the enlarged V_t close-curve on the first side of the applied voltage plane measured after a reset period. The initial point applying the scan high voltage (V_{sch}) on Y electrode after a reset period is located at 150 V of the horizontal axis and 20 V of the vertical axis. In off cell case without an address pulse, when the scan pulse (V_{scl}) on Y electrode is applied, the voltage vector is moved to the outer the threshold voltage curve on a diagonal direction. That is, since the misfiring discharge between the X and Y electrodes is produced, the voltage margin is reduced in the high ΔV_y voltage region.

PROPOSED DRIVING WAVEFORM

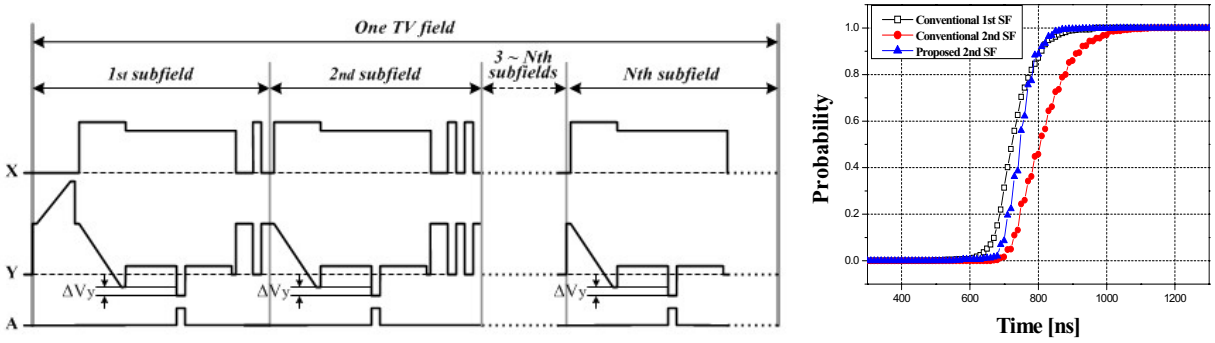
Since the increase in the voltage of ΔV_y on the Y electrode causes a misfiring discharge between the X and Y electrodes, the voltage of ΔV_x (=V_e − V_b) on the X electrode should be controlled properly according to the value of ΔV_y, as shown in the driving waveform of Fig. 5. The V_e voltage plays a role in erasing accumulated wall charges between the X and Y electrodes for preventing misfiring discharge. Fig. 6 (a) shows the enlarged V_t close-curve on the first side of the applied voltage plane measured after the reset period with ΔV_x = 0 V (V_e = 160 V) and ΔV_x = 30 V (V_e = 190 V), respectively. By erasing the wall charges between the X and Y electrodes, as the V_t close-curve is moved to the right direction, the misfiring discharge can be reduced between the X and Y electrodes. Fig. 6 (b) shows the changes in the address voltage margin with an increase in ΔV_y when ΔV_x = 0 and ΔV_x = ΔV_y > 0. As shown in Fig. 6 (b), the address voltage margin is expanded in the case of the high ΔVy condition. When ΔV_y is 30 V, the address voltage can be reduced under 50 V at a scan pulse width of 1.0 μs.

Fig. 7 (a) shows the proposed single-level scan method with identical ΔV_y (=30V) under the fixed negative falling ramp voltage (V_{nf} = - 40) from the first to the N_{th} subfield. Only the first subfield has a rising ramp reset waveform, whereas the other subfields called the subsidiary reset waveform do not [5]. In conventional driving waveform, the same scan low voltage (V_{scl} = -70) is employed during every subfields under the same V_{nf}. When any discharge is not produced in the first subfield, the address discharge time lag in the second subfield was delayed about 200 ns compared with the first subfield as shown in Fig. 7 (b). When the rising and falling ramp waveform is applied during the first subfield, the wall charge is accumulated and redistributed on three electrodes. This wall charges contributed to enhancing the address discharge capability, resulting in producing the address discharge within the scan pulse width of 1 μs successfully. However, in the second subfield without any discharge during the first subfield, the amount of the accumulating wall charges gradually disappeared. This wall charge loss causes the delayed address discharge time lags in the other subfield except the first subfield.



(a) (b)

Fig. 7. (a) Proposed single-level scan method with identical ΔV_y and (b) corresponding discharge probability in second subfield adopting subsidiary reset waveform compared with first subfield adopting main reset waveform.



(a) (b)

Fig. 8. (a) Proposed multi-level scan method with different ΔV_y and (b) corresponding discharge probability in second subfield adopting ΔV_{y2} compared with first and second subfield adopting ΔV_{y1}.

Fig. 8 (a) illustrates the proposed multi-level scan driving waveform with different ΔV_y under the fixed V_{nf} (-40) between the first and the others subfields. The scan low voltages of -70 V and -80 V were applied to the first and the other subfields during an address period, respectively. Fig. 8 (b) shows the address discharge probability in the second subfield compared with the first subfield adopting a ramp reset waveform. As a result, it was found that the address discharge time lags could be reduced as much as about 200 ns.

CONCLUSION

A new driving method can reduce address discharge time lag below 1 μs under a low address voltage (50 V) by high ΔV_y with large voltage margin in the first subfield. A new multi-level scan driving method with different scan low voltages under the same ramp falling voltage is proposed to improve the address discharge characteristics in the subsidiary subfield. When adopting the multi-level scan driving method, the address discharge time lags can be reduced about 200 ns compared with the conventional driving waveform, *i.e.*, the address discharge time lags became almost the same among all subfields.

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