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LETTER

Modified Reset Waveform to Widen Driving Margin under Low Address Voltage in AC-Plasma Display Panel*

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SUMMARY This paper proposes a new reset driving waveform to widen the driving margin under a low address voltage in AC-PDPs. The proposed reset waveform alters the wall charge distribution between the X-Y electrodes by applying an X-ramp bias prior to an address-period, thereby lowering the minimum level of the scan pulse (ΔV_y) during an address-period without any misfiring discharge in the off-cells. When adopting the proposed reset waveform, the address discharge time delay is reduced by about 200 ns at an address voltage of 35 V, while the related dynamic driving margin is wide under a low address voltage condition. The related phenomena are also examined using the V_t close-curve method.

key words: *modified reset waveform, driving margin, low address voltage, V_t close-curves*

1. Introduction

AC-PDPs require low voltage driving to reduce both their power consumption and the driving circuit component cost. In particular, the voltage level of the address pulse needs to be lowered for the application of the single scan driving method for HD (high definition) ac-PDPs or full high-definition (full-HD) ac-PDPs. The overheating of data driver ICs is a more serious problem with the single scan driving method, when compared with the dual scan driving method, due to the increased load, such as the panel capacitance and number of address discharges per single data driver IC. Thus, if the address voltage is reduced, this can significantly reduce the heating problem for the data driver ICs based on a reduction of the address power consumption. However, decreasing the address voltage can cause a reduction in the dynamic driving margin required for the stable driving of millions of micro-discharge cells. Lowering the minimum scan level can help to enhance the address capability of the on-cells, yet this can also simultaneously cause a misfiring discharge in the off-cells. Therefore, the ability to lower the minimum scan level without causing a misfiring discharge in the off-cells and thereby considerably reduce the address voltage without reducing the dynamic voltage margin has been the focus of much research [1]–[4]. In addition, improving the address capability under a wide voltage margin depends heavily on the wall charge distribution among the three electrodes prior to an address discharge, that is, the initialization of the wall charges prior to an address discharge. Thus, although reset waveforms have already been the focus of extensive research [5]–[9], reset waveforms suitable for improving both the address capability and the dynamic driving margin need to be studied further.

Accordingly, this paper proposes a new reset waveform with an X-ramp bias that enables the minimum scan level to be lowered without a misfiring discharge based on altering the wall charges accumulating on the sustain electrodes prior to an address discharge. The effects of the relation between the X-ramp bias and the minimum scan level on the address discharge characteristics are also extensively examined using the V_t close-curve analysis method [3], [4], [9].

2. Experimental SET-UP

Figure 1(a) shows a schematic diagram of the experimental setup used in this study. A 7-in. test panel, photo-sensor amplifier (Hamamatsu, C6386), waveform generator, and power supply were used to measure the address discharge characteristics, including the address time delay relative to the X-ramp bias and minimum scan level, when applying the proposed driving waveform to the 7-in. test panel. The V_t close-curve was also measured to analyze the changes in the wall charges on the three electrodes when adopting the proposed driving waveform. Meanwhile, Fig. 1(b) shows the 2×2 test image pattern used to check for any misfiring discharge by adjacent cells in the 7-in. test panel when applying the proposed driving waveform. The detailed specifications of the 7-in. test panel are listed in Table 1.

Figures 2(a) and (b) show the (a) conventional driving waveform and (b) proposed driving waveform used in this study. For the conventional driving waveform, the rising ramp rate was 1.4 V/μs during the ramp-up period, while the falling ramp rate was −1.5 V/μs during the ramp-down period. For the proposed driving waveform, an X-ramp bias voltage (ΔV_X) ranging from 0 to 50 V was applied to the X electrode for 80 μs after the conventional reset-period, while the rising ramp rate of the X-ramp bias voltage (ΔV_X) ranged from 0 to 0.625 V/μs.

The voltage difference between the minimum scan voltage (V_{scl}) and the negative falling voltage (V_{nf}) is defined as ΔV_y (= V_{nf} - V_{scl}). Thus, the effects of various values of ΔV_y on the address discharge characteristics and corresponding dynamic driving margin relative to the X-ramp

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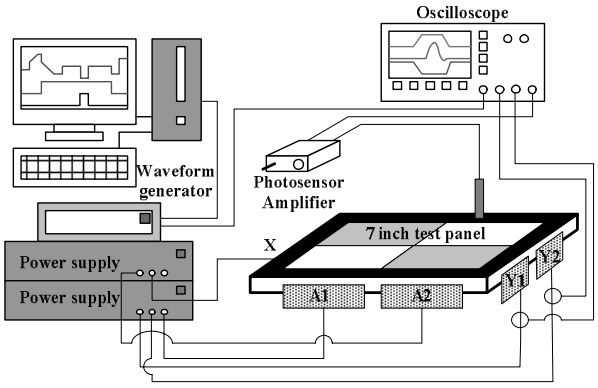
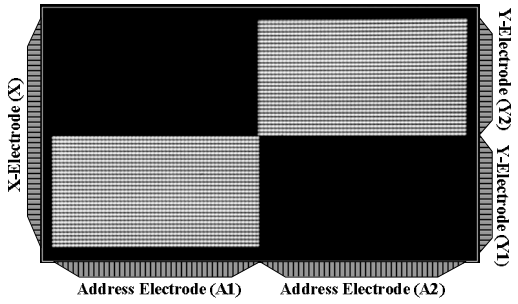


(a)



(b)

Fig. 1 (a) Schematic diagram of experimental setup employed in this study and (b) checker pattern used to check misfiring discharge by adjacent cells in 7-in. test panel.

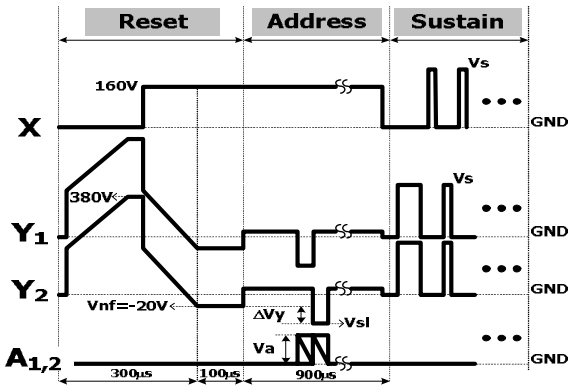
Table 1 Specifications of 7-in. test panel employed in this study.

Front Panel		Rear Panel	
ITO width	310 μm	Barrier rib width	80 μm
ITO gap	60 μm	Barrier rib height	125 μm
Bus width	100 μm	Address width	100 μm
Bus lines		42	
Cell pitch		360μm	
Pressure		400 Torr	
Gas chemistry		Ne-Xe (4%)	
Barrier rib type		Stripe-type rib	
Red phosphor, thickness		$(Y,Gd)BO_3$:Eu, ~13 μm	
Green phosphor, thickness		$(Zn,Mn)_2SiO_4$, ~12 μm	
Blue phosphor, thickness		$(Ba,Eu)MgAl_{10}O_{17}$, ~10 μm	

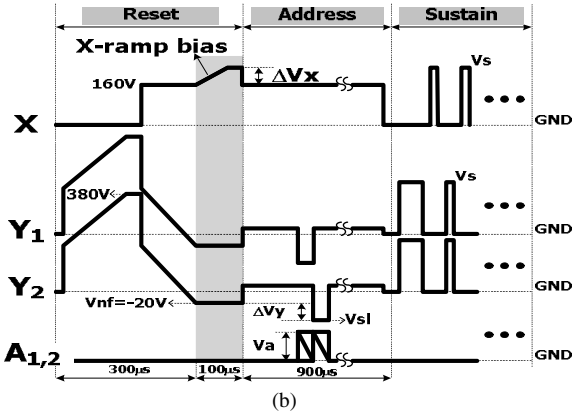
bias voltage (ΔV_X) ranging from 0 to 50 V were examined.

3. Results and Discussion

Figure 3(a) shows the changes in the IR emissions during a reset-period relative to the X-ramp bias (ΔV_X) in Fig. 2 (b) ranging from 0 to 50 V. IR was emitted during the application of the X-ramp bias (ΔV_X), and the IR intensity increased with an increase in the X-ramp bias level up to 50 V. The IR emissions induced by the application of the X-ramp bias represented the redistribution of the accumulated wall charges due to the small variation in the X-Y potential with a minimal slope. As shown in Fig. 3(b), when compared with the conventional case (ΔV_X = 0 V), the V_t close-curve shifted to the right when an X-ramp bias (ΔV_X) of 50 V was



(a)



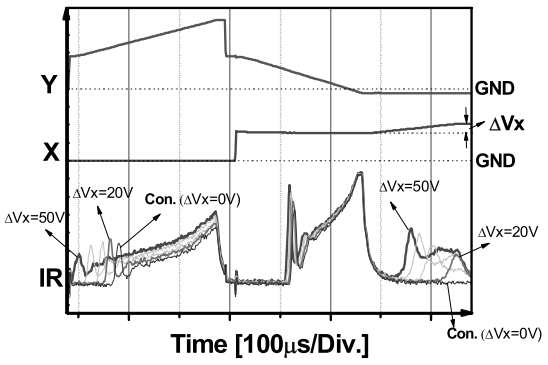
(b)

Fig. 2 (a) Conventional driving waveform and (b) proposed driving waveform used in this study.

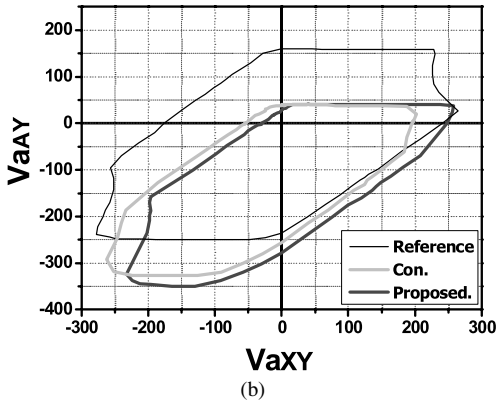
applied prior to the address discharge, indicating that the wall charges accumulating on the Y electrode were erased by the X-ramp bias and accumulated on the X electrode.

Figure 4 shows a schematic diagram of the wall charge distribution on the three electrodes for (a) the conventional and (d) proposed reset waveforms prior to the address discharge. In Figs. 4(a) and (d), ΔV_{WXY} means the variation in the wall voltage between the X-Y electrodes, while ΔV_{WAY} means the variation in the wall voltage between the A-Y electrodes. The method used to determine the values of the wall voltage variations, ΔV_{WXY} and ΔV_{WAY}, for both the conventional and proposed reset waveforms is given briefly as follows [9]. The values of ΔV_{WXY} and ΔV_{WAY} were obtained from the difference between the conventional (or proposed) V_t close-curve in Fig. 3(b) and the reference V_t close-curve in Fig. 3(b) [9].

For the conventional case, as shown in Fig. 4(a), the wall voltage difference between the X-Y electrodes, ΔV_{WXY}, was 25 V, whereas the wall voltage difference between the A-Y electrodes, ΔV_{WAY}, was 120 V. For the proposed case, as shown in Figs. 4(b), (c), and (d), the X-ramp bias voltage was additionally applied to the X electrode after the end of the conventional reset period [Fig. 4(a)] prior to the address discharge. When increasing the X-ramp bias from 0 to 50 V, the wall charges on the Y electrode were erased and accumulated on the X electrode, resulting in a wall voltage dif-



(a)



(b)

Fig. 3 (a) Changes in IR emissions during ramp-period with various X-ramp biases (ΔV_X) when adopting proposed reset waveform in Fig. 2(b), and (b) shift of V_t close-curve, in comparison with conventional case (X-ramp bias, $\Delta V_X = 0$ V), when adopting X-ramp bias (ΔV_X) of 50 V prior to address discharge, where reference means V_t close-curve measured in cells with no wall charges.

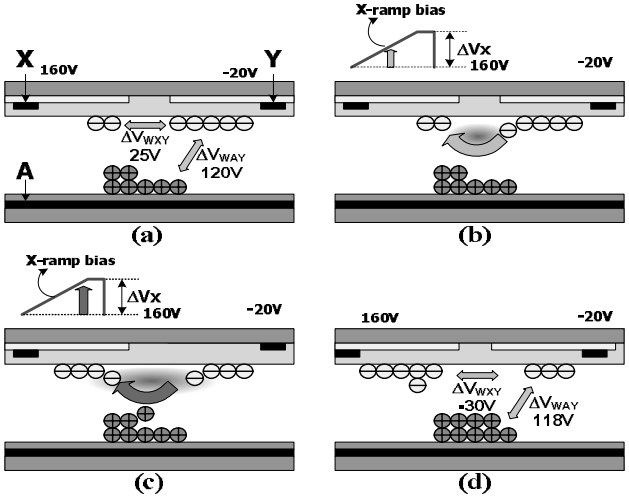


Fig. 4 Wall charge distributions on three electrodes with (a) conventional reset waveform prior to address discharge, (b) and (c) wall charges accumulated during X-ramp bias discharge, and (d) proposed reset waveform prior to address discharge at $\Delta V_X = 50$ V.

ference, ΔV_{WXY} of −30 V for the X-Y electrodes, and wall voltage difference, ΔV_{WAY} of 118 V for the A-Y electrodes, as shown in Fig. 4(d) [9].

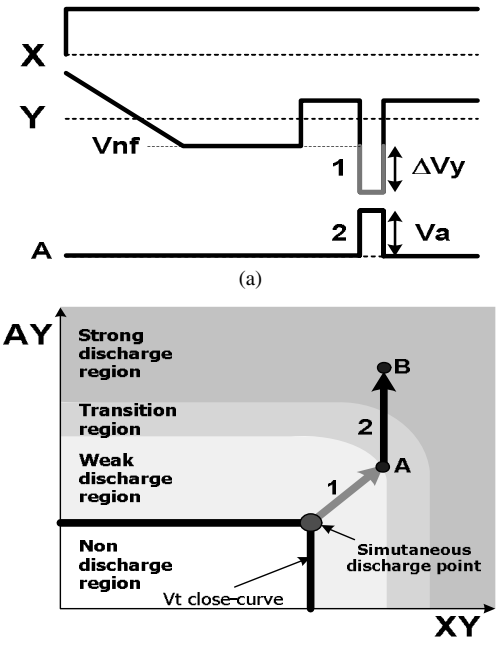


Fig. 5 (a) Application of conventional driving waveform to three electrodes and (b) corresponding cell voltage vector for first quadrant of cell voltage plane in V_t close-curve.

Figures 5(a) and (b) show the application of the conventional driving waveform to the three electrodes and the corresponding cell voltage vector for the first quadrant of the cell voltage plane during an address-period, respectively. It is already well-known that the on- and off-cell voltages determined by the sum of the XY and AY wall voltages and the applied voltages should both be located at a simultaneous discharge point after a reset-period [3]. When applying the voltage of ΔV_y, the cell voltage shifted to point A in the weak discharge region, where it is impossible to produce a strong discharge without applying the address voltage [2], [3]. In contrast, when applying the address voltage (V_a), the cell voltage moved to point B in the strong discharge region.

Figures 6(a) and (b) show the application of the proposed driving waveform to the three electrodes and the corresponding cell voltage vector for the first quadrant of the cell voltage plane, respectively. When applying the X-ramp bias in Fig. 6(a) (arrow 1), the resultant cell voltage vector in Fig. 6(b) moved to point C. With this weak discharge, the wall charges on the Y electrode were erased and accumulated on the X electrode, due to the X-Y discharge induced by the X-ramp bias. When the X-ramp bias was reduced, as shown by arrow 2 in Fig. 6(a), the corresponding cell voltage shifted to the left to point D without any discharge. During an address-period, the cell voltage vector ensuing from the scan pulse exceeded the threshold side in the V_t close-curve and the resultant cell voltage vector (arrow 3) moved to point E, as shown in Fig. 6(b). When the address pulse was applied simultaneously with the scan pulse, the cell voltage vector (arrow 4) shifted upward to point F in the strong discharge region. As shown in Fig. 6(b), the proposed case al-

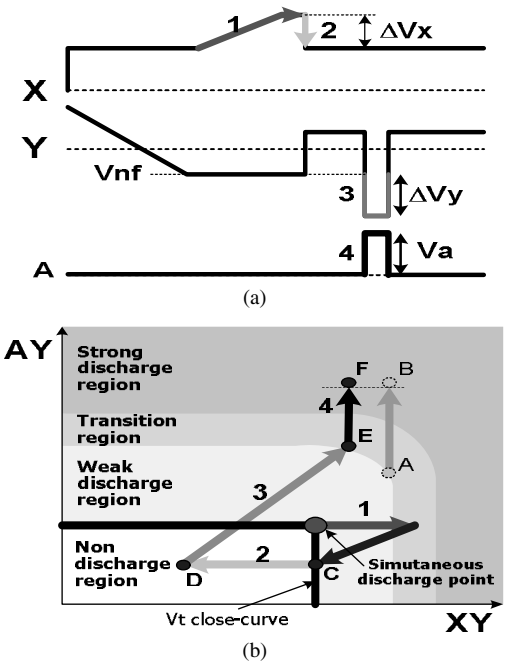


Fig. 6 (a) Application of proposed driving waveform to three electrodes, and (b) corresponding cell voltage vector for first quadrant of cell voltage plane in V_t close-curve.

Table 2 Misfiring discharge phenomena related to ΔV_y and ΔV_X with proposed waveform.

ΔV_y	Conventional	Proposed
0 V ~ 27 V	Non Misfiring	Non Misfiring ($\Delta V_X \geq 0$ V)
30 V	Misfiring	Non Misfiring ($\Delta V_X \geq 10$ V)
35 V	Misfiring	Non Misfiring ($\Delta V_X \geq 20$ V)
40 V	Misfiring	Non Misfiring ($\Delta V_X \geq 30$ V)
44 V	Misfiring	Non Misfiring ($\Delta V_X \geq 50$ V)

lowed a lower minimum scan level [arrow 3 in Fig. 6(b)] to be used as a result of the X-ramp bias, meaning that the minimum scan level, ΔV_y could be lowered without a misfiring discharge. Therefore, the application of a lower scan voltage enabled the address voltage to be reduced, resulting in a successful address discharge under a low address voltage condition without any misfiring discharge.

Table 2 shows the misfiring discharge phenomena related to the low scan voltage (ΔV_y) relative to the ramp-bias voltage (ΔV_X) with the proposed waveform. When the X-ramp bias was applied, the cell voltage vector shifted to point D, located lower left of the simultaneous discharge point. Thus, the minimum scan voltage level of ΔV_y was lowered without a misfiring discharge, as listed in Table 2.

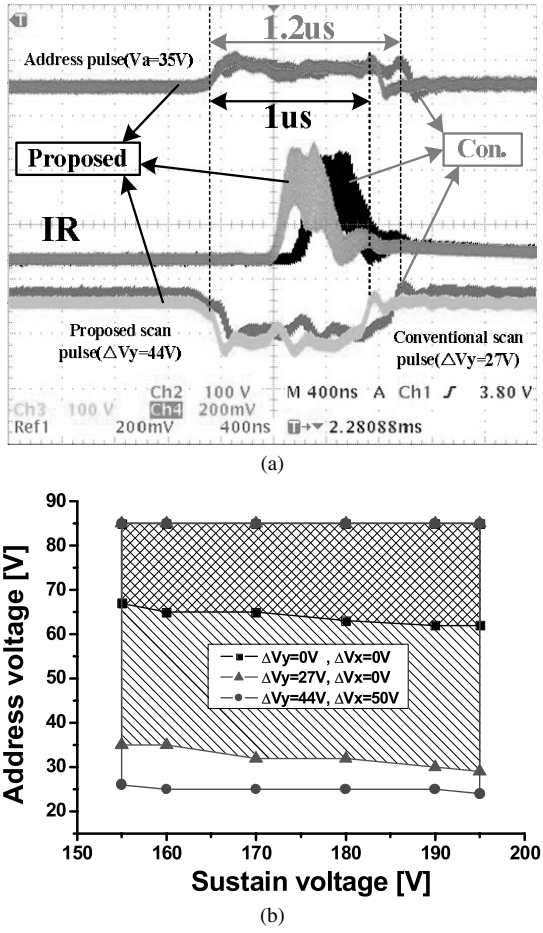


Fig. 7 (a) IR emissions during address discharge characteristics when applying conventional (scan time of 1.2 μs) and proposed (scan time of 1μs) reset waveforms, and (b) changes in dynamic driving margins with various $\Delta V_y$and X-ramp biases (ΔV_X) at scan time of 1.2 μs.

Figure 7(a) shows the IR emissions during an address discharge when applying the conventional and proposed reset waveforms, respectively. When applying the proposed reset waveform, the address discharge delay time was shortened about 200 ns at the same address voltage (35 V). Therefore, the results in Fig. 7(a) confirm that the proposed reset waveform was able to reduce the scan time to about 1 μs. Meanwhile, Fig. 7(b) shows the changes in the dynamic driving margins when applying various ΔV_y and X-ramp biases (ΔV_X). The use of ΔV_y and an X-ramp bias (ΔV_X) in the proposed reset waveform widened the dynamic margin, thereby enabling a low address voltage under wide dynamic margin conditions.

4. Conclusions

This paper proposed a modified rest driving waveform to widen the driving margin under a low address voltage in AC-PDPs. As such, the proposed reset waveform controls the wall charge distribution between the X-Y electrodes by applying an X-ramp bias (ΔV_X) prior to an address-period, thereby lowering the minimum level of the scan pulse (ΔV_y)

and voltage level of the address pulse during an address-period. In addition, the dynamic driving margin, address delay time, and address voltage were examined and compared for both the conventional and proposed reset waveform. By lowering the minimum level of the scan pulse (ΔV_y) and voltage level of the address pulse during an address-period, the proposed reset waveform reduced the address delay time by about 200 ns at an address voltage of 35 V. Furthermore, the proposed reset waveform widened the dynamic driving margin under a low address voltage condition, i.e. the address voltage margin, by about 10 V. Consequently, it is expected that the addition of an X-ramp bias (ΔV_X) will help widen the driving margin under a low address voltage when compared with the conventional reset waveform.

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