

# Improvement of address discharge characteristics based on analysis of weak and strong discharge in AC-PDP

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## Abstract

It is observed that the weak discharge regions for high Xe (20%) content are larger than those of the low Xe (7%) content. This observation allows the higher  $\Delta V_y$  during an address-period without any misfiring discharge for high Xe. In addition, the lower  $V_{x\_add}$  contributes to maximizing the  $\Delta V_y$  throughout the address-period. Therefore, the address discharge delay time is observed to be reduced by about 200 ns.

## 1. Introduction

The high luminance efficiency of current plasma display panel urgently needs to be lowered power consumption for capturing the digital TV consumer market [1]. However, for high luminance efficacy, it is difficult to display the high Xe content conditions under current technology. Moreover, the production of the address discharge is more difficult under high Xe gas mixture conditions. Thus, improving the address discharge characteristics with a high Xe (>10%) gas mixture is very important and strongly depends on how the priming particles and electric field are used in the address discharge [2]. As for the firing voltage with an increase in the Xe content, it is well known that the increase in the Xe concentration results in a reduced effective secondary electron emission coefficient and thus in an increase of the firing voltage [3]. Thus, although driving methods using the electric field and priming particle have already been the focus of extensive research [4...6], the driving methods of high Xe (>20 %) content conditions suitable for improving both the address capability and the stable driving need to be studied further.

Accordingly, this study presents a driving method that compares an additional supply of electric field between the A-Y electrodes during an address period without any misfiring discharge in a 42-in. HD grade PDP with the Xe (7%, 20%) gas mixtures under the ADS driving scheme. Furthermore, the effects of the relation between the electric field and the discharge characteristics on the Xe content conditions are extensively examined using  $V_t$  closed curve analysis method and IR emission.

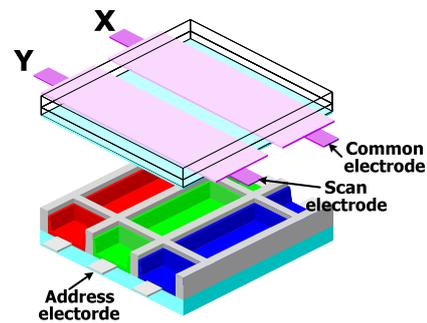


Fig 1. 42-in. HD test panel structure employed in this study.

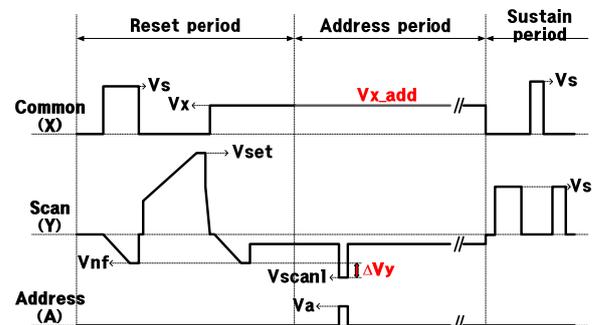


Fig 2. Driving waveform employed in this study.

Table 1. Various bias voltages during address period in Xe 20% test panel

Points	A	B	C	D	E	F
$V_x$ [V]			90			
$V_{x\_add}$ [V]	0	25	50	75	100	125
$V_{nf}$ [V]			-170			
$V_{scan1}$ [V]	-202.5	-200	-197.5	-195	-192.5	-190
$\Delta V_y$ [V]	32.5	30	27.5	25	22.5	20
$V_s$ [V]			205			
$V_a$ [V]			55			

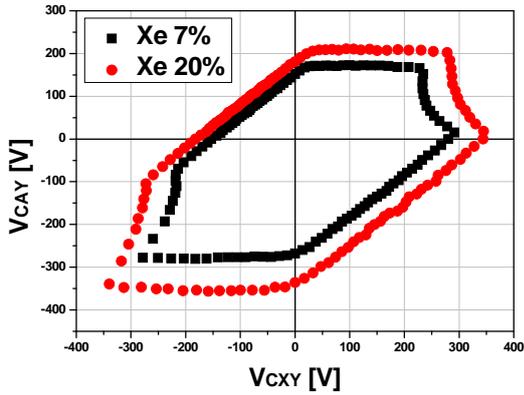


Fig. 3.  $V_t$  closed curves of Xe 7% and Xe 20% 42-in. HD test panel.

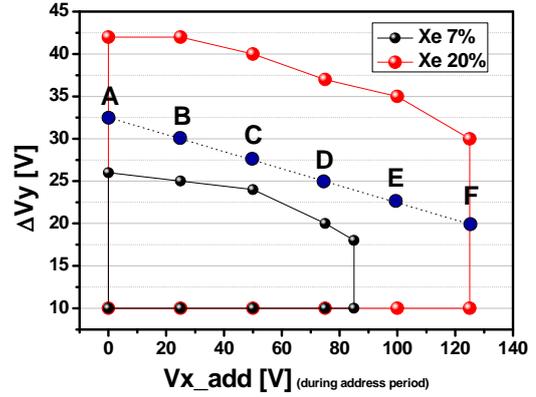
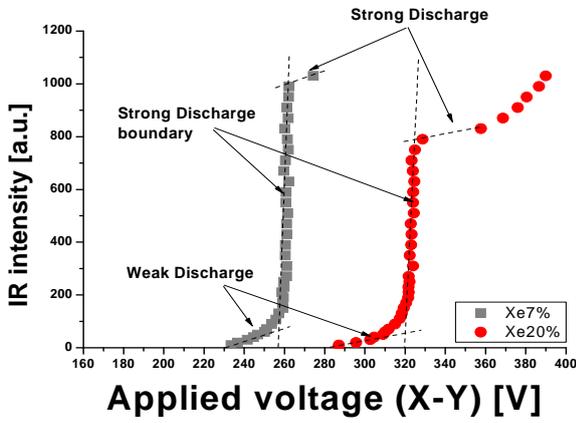
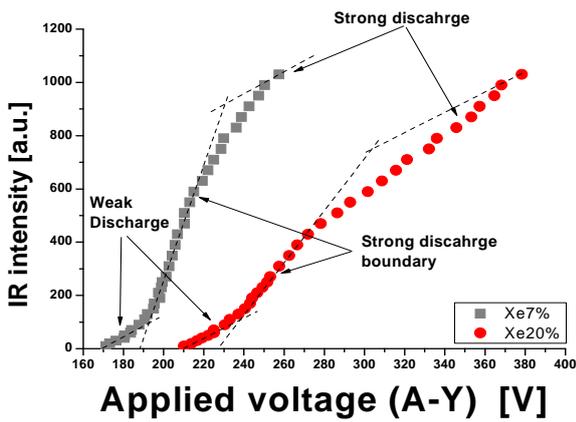


Fig. 5.  $\Delta V_y$  dynamic driving margin by  $V_{x\_add}$  of Xe 7% and Xe 20% 42-in. HD test panel.



(a) X-Y discharge



(b) A-Y discharge

Fig. 4. IR intensity by applied voltage of Xe 7% and Xe 20% 42-in. HD test panel.

## 2. Experimental Setup

Figure 1 shows the conventional 42-in. HD PDP test panel structure. The gas mixture and pressure of test panel were Ne-He-Xe (7% and 20%) and 400 Torr, respectively.

Figure 2 shows the commercial ADS driving waveform for measuring the address discharge characteristics in this study. The detailed values shown in Fig. 2 are given in Table 1.

## 3. Results and Discussion

### 3.1. Weak and Strong Discharge Characteristics

Figure 3 shows the  $V_t$  closed curves of Xe 7% and Xe 20% test panel without initial wall voltage, respectively. The firing voltages are increased by about 60V in the Xe 20% test panel.

Figure 4 shows the changes in IR intensity relative to the applied voltage of Xe 7% and Xe 20% test panels. As shown in Figs. 4 (a) and (b), the applied voltage region of weak IR intensity in Xe 20% content is larger than that in Xe 7% content. As shown in Fig. 4 (b), the IR intensity is slowly generated by increasing the A-Y applied voltage of A-Y discharge region in Xe 20% content. It means that for Xe 20%, the wall charges are slowly accumulated between the A-Y electrodes.

### 3.2. Address Discharge Characteristics

Figure 5 shows the  $\Delta V_y$  dynamic driving margin by various  $V_{x\_add}$  of Xe (7 and 20%) contents without the misfiring discharge. As shown in Fig. 5, the  $\Delta V_y$  dynamic driving

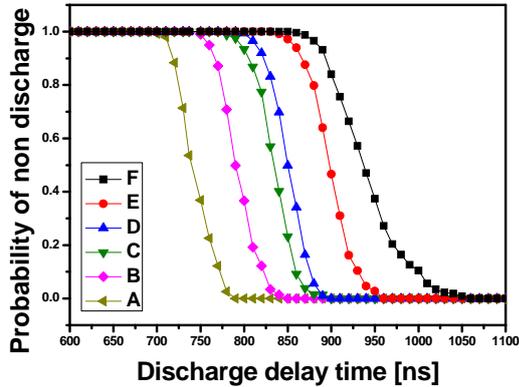


Fig. 6. Probability of non discharge of Xe 20% test panel adopting point (A to F) during address discharge.

Table 2. Address discharge delay time lag in Xe 20% test panel

Points	A	B	C	D	E	F
$T_f$ [ns]	703	750	778	803	843	869
$T_s$ [ns]	47	50	65	54	62	81
$T_d$ [ns] (= $T_f+T_s$ )	750	800	843	857	905	951

margin is wider about 15V under the high Xe (20%) content because the high Xe content has the wider weak discharge region between the A-Y discharge regions in Fig. 4 (b). Furthermore, the  $\Delta V_y$  can be increased by reducing the  $V_{x\_add}$  without any misfiring discharge because the discharges generated in A-Y discharge regions are slower than those in X-Y discharge.

Figure 6 shows the probability of non discharge during the address discharge. As shown in Fig. 6, the address discharge delay times are reduced by higher  $\Delta V_y$  (point A) without misfiring discharge. Table 2 show the address discharge delay time lags by various  $V_{x\_add}$  in Xe 20% test panel. As shown in Table 1, the address discharge delay times ( $T_d$ ) are reduced by about 200 ns by decreasing  $V_{x\_add}$  (Point F→A) with higher  $\Delta V_y$ . Therefore, the adjustable control about  $V_{x\_add}$  and  $\Delta V_y$  can realize a high speed addressing under high Xe(20%) content.

#### 4. Conclusions

It is observed that the weak discharge regions of the high Xe (20%) content are larger than those of the low Xe (7%) contents. Accordingly, the higher  $\Delta V_y$  during an address-period can be applied without any misfiring discharge. In addition, the lower  $V_{x\_add}$  contributes to maximizing the  $\Delta V_y$  throughout the address-period. As a result, the address discharge delay time ( $T_d$ ) is observed to be reduced by about 200 ns. Thus, it is expected that these experimental results will help reduce the problem of unstable address discharge in high Xe (>20%) PDPs.

#### 5. References

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