High-Speed Driving Method Using Bipolar Scan Waveform in AC Plasma Display Panel

Heung-Sik Tae, *Senior Member, IEEE*, Soo-Kwan Jang, Ki-Duck Cho, and Ki-Hyung Park

***Abstract*—This paper proposes a new high-speed driving method using the bipolar scan waveform with a scan width of 1 μs in an ac-plasma display panel. The bipolar scan waveform in an address period consists of a two-step pulse with two different polarities, i.e., a forward scan pulse with a negative polarity and reverse scan pulse with a positive polarity, which can produce two address discharges, including a primary address discharge for generating wall charges and secondary address discharge for accumulating wall charges. To produce the fast address discharge stably using the bipolar scan pulse during an address period, a new reset waveform is designed based on a V_t close curve analysis, and the address discharge characteristics examined under various reset and address waveforms. As a result of adopting the proposed driving method, a high-speed address with a scan width of 1 μs is successfully obtained when using a checkered pattern on a 4-in test panel.**

***Index Terms*—Bipolar scan waveform, forward scan pulse, high-speed address, misfiring discharge, reverse scan pulse, V_t close (VTC) curve analysis.**

I. Introduction

A FAST address technique is the one of the most important issues for current plasma display panel (ac-PDP) technology as regards realizing a low cost and high-class display device. A fast address can improve the image quality, luminance, contrast ratio, and peak luminance, and so on [1], however, producing an address discharge within a very short period, such as 1 μs, is difficult due to the time needed to generate and accumulate the wall charges for the subsequent sustain discharge. A lot of research has already been focused on the development of a fast address technique [2]–[6], including a previous report by the present authors on the basic concept of a bipolar scan waveform that can considerably reduce the address time [7]. The bipolar scan waveform uses a two-step scan pulse with two polarities, which separates the conventional address discharge into two different discharge modes: a wall charge generation mode produced by the first-step scan pulse with a negative polarity, i.e., the forward scan pulse, and a wall charge accumulation mode produced by the second-step scan pulse with a positive polarity, i.e., the reverse scan pulse [7]. Since the scan time is only determined by the wall charge generation mode, this bipolar scan waveform enables a high-speed address. However, with this driving method, since the reverse scan pulse with a positive polarity produces another discharge between the common and scan electrodes to accumulate the wall charges, a negative bias is applied to the common electrode, unlike the conventional driving method that applies a positive bias to the common electrode. Consequently, the conventional reset waveform is not applicable to the proposed high-speed driving method.

Accordingly, this paper proposes a high-speed driving method using the bipolar scan waveform for a fast address. A new reset waveform applicable to the bipolar scan waveform is designed based on the V_t close curve (hereinafter VTC curve) analysis suggested by Sakita *et al.* [8]. The misfiring problems are examined using the voltage slope during the transition from the forward scan pulse to the reverse scan pulse. By measuring the VTC curve, the various voltage parameters, such as the scan ramp set-down voltage V_{SD}, positive *X*-bias voltage, V_B for the reset waveform, negative *X*-bias voltageV_Z, reverse scan pulse V_R, and address pulse V_A for the bipolar scan waveform, are optimized to improve the fast address discharge characteristics without any misfiring discharge when using a checkered pattern on a 4-in test panel.

II. Proposed High-Speed Address Method Using Bipolar Scan Waveform

Fig. 1(a) shows the electrode configuration used in the 4-in test panel, while Fig. 1(b) shows the proposed driving waveforms using a bipolar scan pulse for a high-speed address in an ac-PDP. The detailed panel specifications are listed in Table I. In the proposed driving waveforms, unlike the conventional scan waveform, a bipolar scan pulse with two different polarities is applied to the *Y* electrode during an address period. As such, the address speed is determined by the width of the forward scan pulse with a negative polarity, that is, the first-step pulse in the bipolar scan waveform, while the address capability for the subsequent stable sustain discharge is determined by the reverse scan pulse with a positive polarity, that is, the second-step pulse in the bipolar scan waveform. In this case, a new reset waveform suitable for the bipolar scan waveform needs to be designed. The detailed operational and design principles for the bipolar scan waveform and corresponding reset waveforms are given in the following.

A. Operational Principle of Bipolar Scan Waveform During Address-Period

The main function of an address discharge is to accumulate the sufficient amount of wall charges on the *X* and *Y* electrodes

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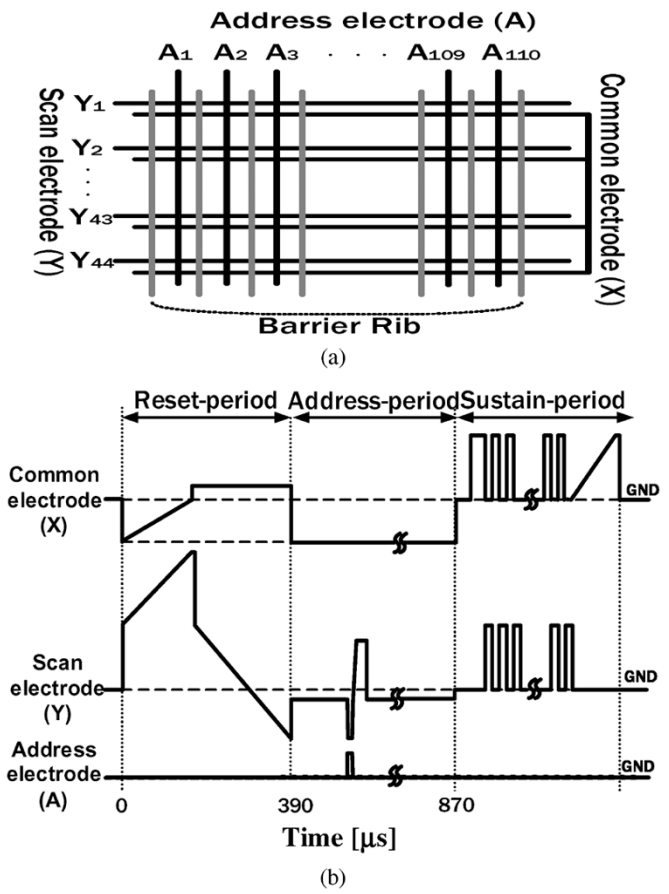

Fig. 1. (a) Electrode configuration used in test panel and (b) proposed driving waveforms using bipolar scan pulse for high-speed address in ac-PDP.

TABLE I
DETAILED SPECIFICATIONS OF TEST PANEL

Specifications of test panel	
Pixel pitch	1.08 mm
Thickness of dielectric layer	30 μm
Rib Height	130 μm
Gas mixture	Ne –Xe (4 %), 400 Torr
ITO width	310 μm
ITO gap	60 μm
Address electrode width	100 μm

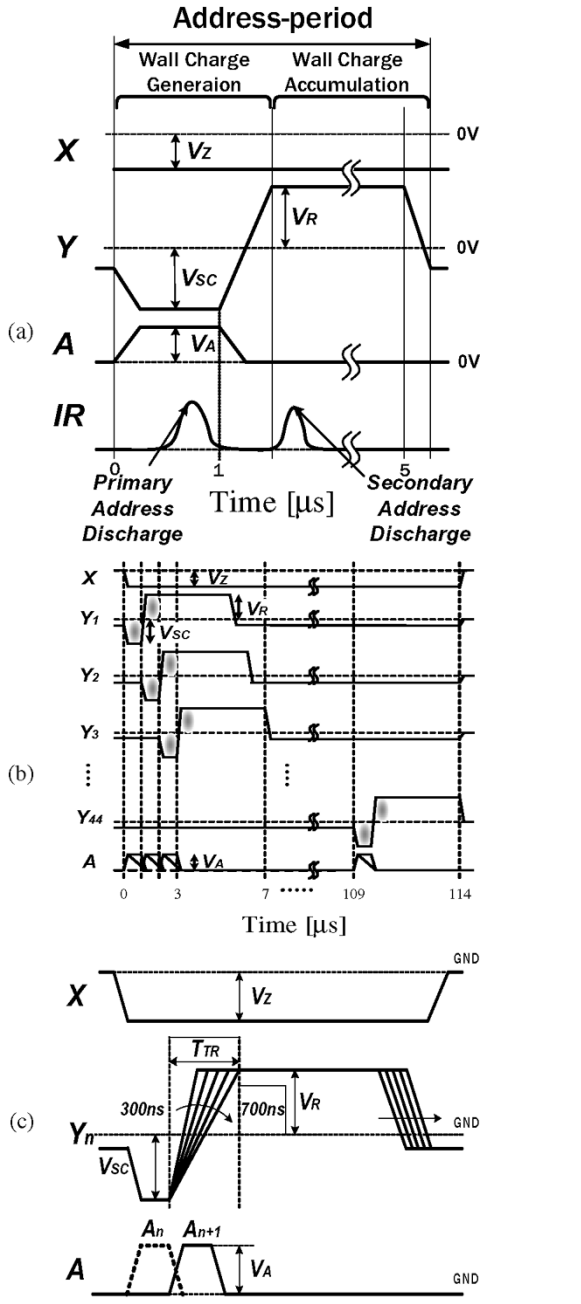

Fig. 2. (a) Bipolar scan waveform, (b) address procedure using bipolar scan waveform during address period, and (c) misfiring discharge problem.

for the stable sustain discharge by producing the address discharge between the *Y* and *A* electrodes. In the conventional address waveform, the formative and statistical time lags of address discharge should be considered for determining the width of address pulse, because the wall charge generation and accumulation process should be completed during the address discharge, that is, within the width of address pulse. However, in the proposed bipolar scan waveform, the one conventional address discharge is separated into the two address discharges, such as the first address discharge produced between the *Y* and *A* electrodes and the second address discharge produced between the *X* and *Y* electrodes. In this case, the second address discharge, hereinafter called the "secondary address discharge" can be produced only in the cells where the first address discharge, hereinafter called the "primary address discharge" has been produced, implying that no secondary address discharge can be produced without the primary address discharge even if the driving voltages for the second address discharge are applied to the *X* and *Y* electrodes. The primary address discharge just plays a role in generating the wall charges, but not in accumulating the wall charges. Consequently, in the proposed bipolar scan waveform for the fast address procedure, the formative and statistical time lags of address discharge need not be considered for determining the width of address pulse.

Fig. 2(a) shows the voltage waveforms and corresponding IR emission when applying the bipolar scan waveform to the *Y* electrode. In Fig. 2(a), the first-step pulse, with a negative

amplitude of $V_{\rm SC}(<0)$, in the bipolar scan waveform is a forward scan pulse that is similar to the conventional scan pulse applied to the *Y* electrode. As shown in Fig. 2(a), the first address discharge, that is, the primary address discharge, is produced between the *Y* and *A* electrodes by applying both the forward scan and address pulses. Yet, since the main function of the forward scan pulse is just to generate wall charges in combination with the application of the address pulse, V_A, during an address period, its width can be reduced to within 1 μs. Thus, given that the total address time is determined by the width of the forward scan pulse in the bipolar scan waveform, it is expected that the total address time can be reduced considerably. The second-step pulse, with a positive amplitude of $V_R(>0)$, in the bipolar scan waveform is a reverse scan pulse and produces the second address discharge, that is, the secondary address discharge, with the application of the negative *X*-bias voltage of $V_Z(<0)$. As such, the main function of the reverse scan pulse is to accumulate wall charges by producing another discharge between the *Y* and *X* electrodes immediately after the primary address discharge is induced by the forward scan pulse. Thus, unlike the conventional case, the negative *X*-bias of $V_Z(<0)$ is applied to the *X* electrode during an address period, as shown in Fig. 2(a). The stable production of the first sustain discharge in a sustain-period depends strongly on the secondary address discharge that can be considered like the first sustain discharge produced during an address period. Consequently, the basic concept of the proposed bipolar scan waveform is to separate the conventional one address discharge into two address discharges: i.e., a primary address discharge that generates wall charges and secondary address discharge that accumulates wall charges. Note that the secondary address discharge can be produced even at a relatively low sustain gap voltage due to the presence of the space charges still remaining after the primary address discharge. Hence, the secondary address discharge was only produced in the cells where the primary address discharge was produced. Fig. 2(b) shows the address procedure carried out by the bipolar scan waveform from scan line 1 to 44. For the bipolar scan waveform, the forward scan pulse is not overlapped with any other address pulse, whereas the reverse scan pulse is overlapped with another address pulse, as shown in Fig. 2(b). Thus, this type of address procedure is a kind of parallel processing for a high-speed address, making it very important to avoid any misfiring discharge during the overlapping. As shown in Fig. 2(c), since the voltage polarity of the reverse scan pulse $V_R(>0)$ is the same as that of the address pulse $V_A(>0)$ a misfiring discharge can be prevented during overlapping on condition that the voltage slope for the transition from the forward to the reverse scan pulse is properly controlled. That is, misfiring problems depend strongly on the transition time $T_{\rm TR}$ of the bipolar scan pulse from the forward to the reverse scan pulse. The specific condition to prevent a misfiring discharge will be discussed later.

B. Design of Reset Waveform Suitable for Bipolar Scan Waveform Based on V_t Close Curve Analysis

Fig. 3 shows the new reset waveform suitable for the bipolar scan waveform based on the VTC curve measured from the test panel, where the VTC curve is defined as the closed curve

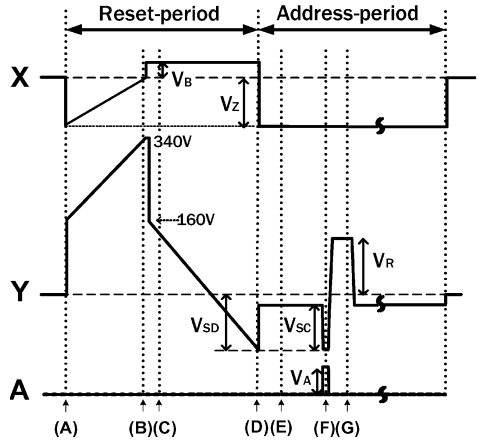

Fig. 3. Proposed reset waveform suitable for new bipolar scan pulse for high-speed address of ac-PDP where V_B is positive *X*-bias voltage, $V_{\rm SD}$ is scan ramp set-down voltage, V_Z is negative X-bias voltage, $V_{\rm SC}$ is forward scan pulse, V_Z is reverse scan pulse, and V_A is address pulse.

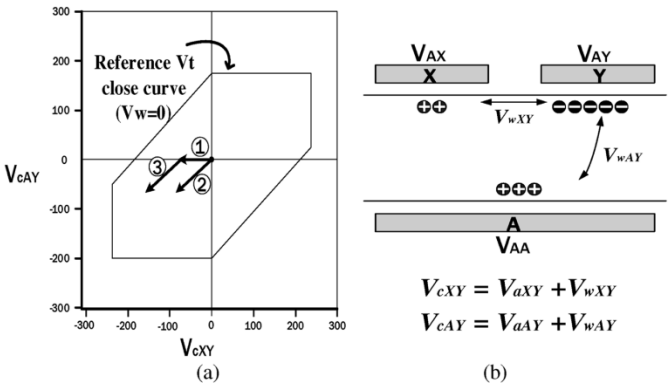

Fig. 4. (a) Reference VTC curve with six threshold firing voltage sides on cell voltage plane measured for cells without any wall charges, and (b) relations among cell voltage $(V_{\rm cXY}, V_{\rm cAY})$, applied voltage $(V_{\rm aXY}, V_{\rm aAY})$, and wall voltage $(V_{\rm wXY}, V_{\rm wAY})$.

formed by the cell voltage vector on the cell voltage plane when the break down condition is satisfied [8]. Fig. 4(a) shows the reference VTC curve with six threshold firing voltage sides on the cell voltage plane measured for the cells without any wall charges where the horizontal axis represents the cell voltage between the *X* and *Y* electrodes $V_{\rm cXY}$ and the vertical axis represents the cell voltage between the *A* and *Y* electrodes, $V_{\rm cAY}$. As shown in Fig. 4(b), the cell voltage $V_{\rm cXY}$ is a sum of $V_{\rm aXY}$ and $V_{\rm wXY}$, where $V_{\rm aXY}$ is a voltage externally applied between the *X* and *Y* electrodes and $V_{\rm wXY}$ is a wall voltage induced by the wall charges accumulating on the *X* and *Y* electrodes. In the same manner, the cell voltage, $V_{\rm cAY}$ is a sum of $V_{\rm aAY}$ and $V_{\rm wAY}$, where $V_{\rm aAY}$ is a voltage externally applied between the *A* and *Y* electrodes and $V_{\rm wAY}$ is a wall voltage induced by the wall charges accumulating on the *A* and *Y* electrodes. In the VTC curve, the voltage applied to the *Y* electrode (hereinafter the *Y* -voltage) is a reference voltage, and as such the following voltage equations are satisfied:

$$\mathbf{V}_{\rm cXY} = \mathbf{V}_{\rm aXY} + \mathbf{V}_{\rm wXY}, \mathbf{V}_{\rm aXY} = \mathbf{V}_{\rm aX} - \mathbf{V}_{\rm aY}$$
$$\mathbf{V}_{\rm wXY} = \mathbf{V}_{\rm wX} - \mathbf{V}_{\rm wY}, \mathbf{V}_{\rm cAY} = \mathbf{V}_{\rm aAY} + \mathbf{V}_{\rm wAY}$$
$$\mathbf{V}_{\rm aAY} = \mathbf{V}_{\rm aA} - \mathbf{V}_{\rm aY}, \mathbf{V}_{\rm wAY} = \mathbf{V}_{\rm wA} - \mathbf{V}_{\rm wY}$$

where $V_{\mathrm{aX}}, V_{\mathrm{aY}}$, and V_{aA} are the voltages externally applied to the *X*, *Y*, and *A* electrodes, respectively, and $V_{\mathrm{wX}}, V_{\mathrm{wY}}$, and V_{wA} are the wall voltages due to the wall charges accumulating on the *X, Y*, and *A* electrodes, respectively. In Fig. 4(a), the region within the VTC curve indicated the nondischarge region, whereas the region outside the VTC curve indicated the discharge region. Since the VTC curve in Fig. 4(a) was measured under the zero wall voltage condition ($V_{\mathrm{wX}} = V_{\mathrm{wY}} = V_{\mathrm{wA}} = 0$ V), the cell voltage was equal to the applied voltage, i.e., $V_{\mathrm{cXY}} = V_{\mathrm{aXY}}, V_{\mathrm{cAY}} = V_{\mathrm{aAY}}$. The case ① in Fig. 4(a) designated the cell voltage vector when applying the V_{aX1} ($<V_f$: a firing voltage) < 0 V, and $V_{\mathrm{aY1}} = V_{\mathrm{aA1}} = 0$ V. The case ② in Fig. 4(a) designated the cell voltage vector when applying the $V_{\mathrm{aY2}}(< V_f) > 0$ V, and $V_{\mathrm{aX2}} = V_{\mathrm{aA2}} = 0$ V. The case ③ in Fig. 4(a) designated the cell voltage vector when applying the $V_{\mathrm{aX3}}(< V_f) = V_{\mathrm{aX1}} + \triangle V_{\mathrm{aX3}}(< 0V), V_{\mathrm{aY3}}(< V_f) > 0$ V, and $V_{\mathrm{aA3}} = 0$ V. The exceeding of the VTC curve in the cell voltage plane strongly depends on how to apply the voltages to the three electrodes in addition to the wall charge states among the three electrodes. Since the V_{cXY} and V_{cAY} are equal to the V_{aXY} and V_{aAY}, respectively, under zero wall voltage condition, the reference VTC curve, V_{Ct1} in the cell voltage plane, shown in the measured curve of Fig. 4(a), can be also expressed in the reference VTC curve, V_{At1} in the applied voltage plane where the horizontal axis represents the V_{aXY} and the vertical axis represents the V_{aAY}. In this case (case ①), $V_{\mathrm{Ct1}} = V_{\mathrm{At1}}$, which provides information about a firing voltage under zero wall voltage vector. If the applied voltage satisfies a firing condition, the discharge is initiated, so that the wall charges start to be accumulated on the three electrodes, and the resultant VTC curve, V_{At2} is shifted on the applied voltage plane. In this case (case ②), the following relation is satisfied: $V_{\mathrm{At2}} = V_{\mathrm{Ct1}} - \nabla V_w$ where the value of V_{Ct1} is obtained from case ①, and the V_{At2} is obtained by measuring the applied voltage at the firing discharge condition. Accordingly, to measure the wall voltage induced by the wall charge accumulation, the changed VTC curve needs to be measured again in the applied voltage plane. The exact value of the wall voltage can be obtained by comparing the reference VTC curve with the changed VTC curve induced by the wall charge accumulation in the applied voltage plane.

Fig. 5(a) and (c) shows the schematic diagrams of the measured VTC curves prior to the reset-period for both the (a) on- and (c) off-cells relative to the reference VTC curves measured from the cells without any wall charges, respectively, on the applied voltage plane. On the applied voltage plane V_{aXY} and V_{aAY}, the measured VTC curves were shifted due to the change in the initial wall voltage. As shown in Fig. 5(a) and (c), the reference VTC curves were fixed for both on- and off-cells because they were measured from the cells without any wall charges, whereas the measured VTC curves for both the on- and off-cells were sifted to the lower-left direction $\triangle V_w$ with respect to the reference VTC curves, respectively. Here, the VTC curves measured prior to the reset-period (at point A in Fig. 3) provide information about the initial wall voltage obtained from the variations in the wall charges among the three electrodes due to the erase sustain discharge for the on-cells or due to the reset discharge during the ramp-down period for the off-cells. The total wall voltage variation $\triangle V_w$ in Fig. 5(a) and (c) was made by the

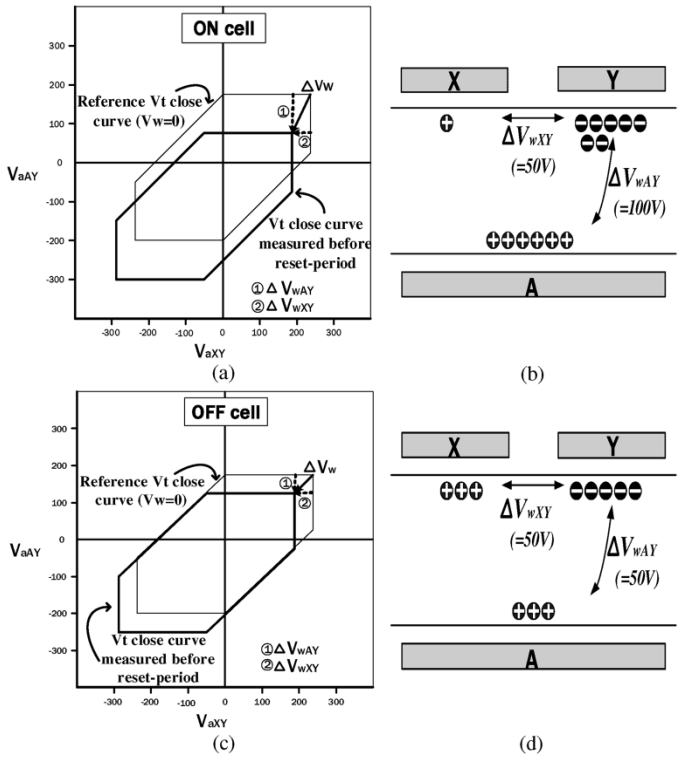

Fig. 5. (a) and (c) Schematic diagrams of VTC curves measured prior to reset-period from (a) on- and (c) off-cells relative to reference VTC curves measured from cells without any wall charges, respectively, and (b) and (d) measured wall voltages, $\triangle V_{\mathrm{wXY}}$ and $\triangle V_{\mathrm{wAY}}$ for (b) on- and (d) off-cells.

sum of the variation in the wall voltage between the *A* and *Y* electrodes, $\triangle V_{\mathrm{wAY}}$ and the variation in the wall voltage between the *X* and *Y* electrodes $\triangle V_{\mathrm{wXY}}$. Accordingly, as shown in Fig. 5(b) and (d), the measured wall voltages $\triangle V_{\mathrm{wXY}}$ and $\triangle V_{\mathrm{wAY}}$ were 50 and 100 V for the on-cells, respectively, whereas the measured wall voltages $\triangle V_{\mathrm{wXY}}$ and $\triangle V_{\mathrm{wAY}}$ were 50 and 50 V for the off-cells, respectively.

The measured hexagonal-shaped VTC curve shown in Fig. 4(a) provides information about the firing voltage condition among the three electrodes in the test panel: the firing voltage between the *Y* and *A* electrodes was 170 V under an MgO cathode condition and 220 V under a phosphor cathode condition, whereas the firing voltage between the *Y* and *X* electrodes was 220 V. Fig. 6(a)–(c), and (d) shows the trajectories for the cell and wall voltages according to the voltage level applied during the reset- and address periods on the cell voltage plane based on the VTC curve measured from the test panel. The changes in the cell and wall voltages for both the on- and off-cells according to the driving waveform in Fig. 3 are described by the VTC curve on the cell voltage plane as follows.

1) Ramp Set-Up Region in Reset-Period (A–B Region in Fig. 3): Prior to the reset-period after a sustain-period, the wall voltage for the off-cells continued in the same state as that after the reset process, as there was no address discharge. Accordingly, the scan ramp set-down voltage V_{SD}, and positive *X*-bias voltage, V_B in the reset waveform determined the initial wall voltage for the off-cells. Meanwhile, the erase pulse applied to the *X* electrode after applying the previous sustain

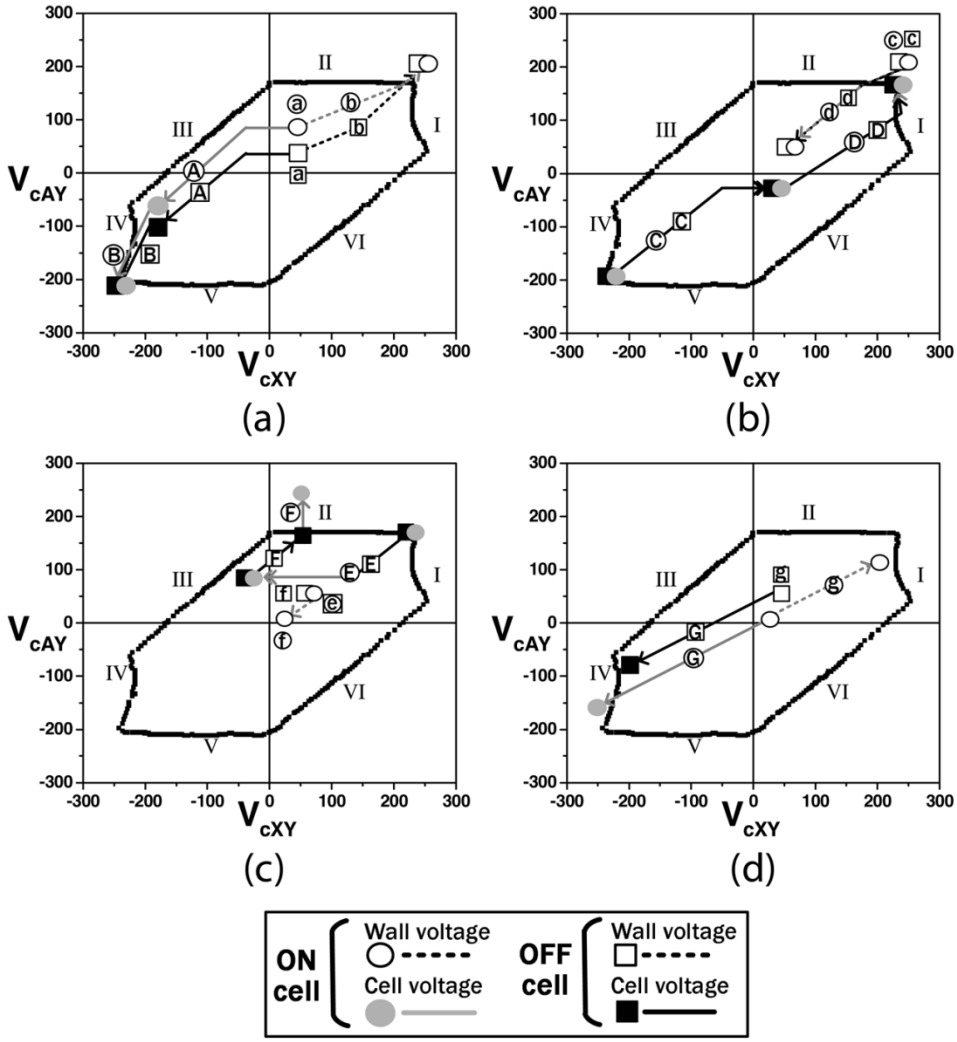

Fig. 6. Trajectories of cell voltage and wall voltage on cell voltage plane relative to applied voltages during reset- and address periods. (a) Set-up region. (b) Set-down region. (c) Wall-charge generation region. (d) Wall-charge accumulation region, where I: V_{tXY} (=Discharge start threshold cell voltage between *X* and *Y*), II: V_{tAY} (=Discharge start threshold cell voltage between *A* and *Y*), III:V_{tAX} (=Discharge start threshold cell voltage between *A* and *X*), IV: V_{tYX} (= Discharge start threshold cell voltage between *Y* and *X*), V: V_{tYA} (= Discharge start threshold cell voltage between *Y* and *A*), and VI: V_{tXA} (= Discharge start threshold cell voltage between *X* and *A*).

pulse to the *Y* electrode determined the initial wall voltage for the on-cells. As a result of the wall voltage measurement in Fig. 5(a) and (c), the initial wall voltages were located at different position for the on- and off-cells, respectively, as shown in points ⓐ and [a] of Fig. 6(a), where the points ⓐ and [a] designated the positions of initial wall voltages on the cell voltage plane prior to the reset period for the on- and off-cells, respectively. When +160 V and V_Z (= − 80 V) were applied to the *Y* and *X* electrodes [(A) in Fig. 3], respectively, the cell voltages moved to the lower-left (a→ path A), yet the wall voltages did not change, since there was no discharge, and the resultant initial wall voltage positions for the on- and off-cells did not change, as shown in points ⓐ and [a] of Fig. 6(a). Here, the path Ⓐ designated the change in the cell voltage, $\triangle V_{\mathrm{cXY}}(= -190\ V)[= V_{\mathrm{aXY}}(= -240\ V) + V_{\mathrm{wXY}}(= 50\ V)]$, and $\triangle V_{\mathrm{cAY}}(= -60\ V)[= V_{\mathrm{aAY}}(= -160\ V) + V_{\mathrm{wAY}}(= 100\ V)]$ for the on- cells, whereas the path [A] designated the change in the cell voltage, $\triangle V_{\mathrm{cXY}}(= -190\ V)[= V_{\mathrm{aXY}}(= -240\ V) + V_{\mathrm{wXY}}(= 50\ V)]$, and $\triangle V_{\mathrm{cAY}}(= -110\ V)[= V_{\mathrm{aAY}}(= -160\ V) + V_{\mathrm{wAY}}(= 50\ V)]$ for the off-cells. After that, the scan ramp voltage increased slowly from +160 toward +340 V and the negative ramp *X*-bias voltage was reduced to zero voltage during the ramp-up period [(B) in Fig. 3]. For the on-cells, the change in the cell voltage, $\triangle V_{\mathrm{cXY}}$ at the path Ⓑ reached −370 V because it was a sum of the applied additional voltage, $\triangle V_{\mathrm{aXY}}(= -180\ V)$ and the change in the cell voltage, $\triangle V_{\mathrm{cXY}}(= -190\ V)$ at the path Ⓐ, and the change in the cell voltage, $\triangle V_{\mathrm{cAY}}$ at the path Ⓑ reached −240 V because it was a sum of the applied additional voltage, $\triangle V_{\mathrm{aAY}}(= -180\ V)$ and the change in the cell voltage, $\triangle V_{\mathrm{cAY}}(= -60\ V)$ at the path Ⓐ. For the off-cells, the change in the cell voltage, $\triangle V_{\mathrm{cXY}}$ at the path [B] reached -370 V because it was a sum of the applied additional voltage, $\triangle V_{\mathrm{aXY}}(= -180\ V)$ and the change in the cell voltage, $\triangle V_{\mathrm{cXY}}(= -190\ V)$ at the path [A], and the change in the cell voltage, V_{cAY} at the path [A] reached −270 V because it was a sum of the applied additional voltage, $\triangle V_{\mathrm{aAY}}(= -180\ V)$ and the change in the cell voltage, $\triangle V_{\mathrm{cAY}}(= -90\ V)$ at the path [A]. Accordingly, the resultant cell

voltages for both the on- and off-cells exceeded one side [V_{tYX} (Ⅳ: *Y–X* discharge region)] of the VTC curve, which meant that a weak reset discharge was produced between the *Y* and *X* electrodes. During the ramp-up period, the negative ramp *X*-bias voltage (slope: about 0.4 V/μs) was applied to the *X* electrode to produce a surface discharge instead of a plate gap discharge for a stable reset discharge by prohibiting a phosphor-cathode discharge condition under a low background luminance. In the *Y–X* discharge region, the cell voltage reached the *X–Y* and *Y–A* simultaneous discharge point [= intersection point of V_{tYX}(Ⅳ) and V_{tYA}(Ⅴ: *Y–A* discharge region)] on the VTC curve through several weak discharges during the ramp-up period. The scan ramp set-up voltage increased until the cell voltages for both the on- and off-cells reached the simultaneous discharge point. In this case, the scan ramp set-up voltage was 340 V. That is to say, the final destination in paths Ⓑ and Ⓑ reached the same point, i.e., the *X–Y* and *Y–A* simultaneous discharge point on the VTC curve irrespective of the on- and off-cells, as shown in Fig. 6(a). When the *Y–X* discharge occurred, the wall voltages moved to the upper-right based on a slope of $^1/_2$, because their polarity was opposite to that of the applied voltage. When the *Y–X* and *Y–A* simultaneous discharges occurred, the wall voltages moved to the upper-right based on a slope of 1. The off-cells reached the *Y–X* and *Y–A* simultaneous discharge point ahead of the on-cells, thereby moving the final wall voltages to the same point (a→ path b) irrespective of the on- or off-cells, as shown on the right-side of Fig. 6(a). The paths ⓑ and ⓑ designated the changes in the wall voltages for the on- and off-cells during the application of the ramp-up voltage, respectively, and their directions were opposite to the polarities of the applied voltages, respectively. In this case, the changes in the wall voltages for the on- and off-cells were measured by the method described in Fig. 5(a) and (c).

2) Ramp Set-Down Region in Reset-Period (C–D Region in Fig. 3): When the ramp set-up voltage was abruptly reduced from +340 to +160 V and the *X*-bias voltage V_B increased from 0 to +50 V [(C) in Fig. 3], the cell voltages moved to the upper-right (path C), yet the wall voltages did not change, since there was no discharge, as shown in Fig. 6(b). Here, the paths Ⓒ and ⓒ designated the change in the cell voltage for the on- and off-cells caused by the variations in the *X*- and *Y*-voltages. The points Ⓒ and ⓒ designated the wall voltage positions for the on- and off-cells, respectively, which were located unchanged due to the absence of discharge. Thereafter, when the ramp set-down voltage decreased from +160 V to-V_{SD} [(D) in Fig. 3], the cell voltages exceeded V_{tXY} (Ⅰ: *X–Y* discharge), resulting in a weak *X–Y* discharge. On exceeding V_{tXY}(Ⅰ), a weak discharge caused a small change in the wall charges, such that the cell voltage returned to the higher point on the side [V_{tXY}(Ⅰ)] of the VTC curve. At this time, as the ramp set-down voltage was reduced to a lower level, the cell voltage exceeded V_{tXY}(Ⅰ) again, resulting in a small change in the wall charge and in the return to a higher point on the side [V_{tXY}(Ⅰ)] of the VTC curve [8]. In this manner, the resultant cell voltages moved to the *X–Y* and *A–Y* simultaneous discharge point [= intersection point of V_{tXY}(Ⅰ) and V_{tAY} (Ⅱ: *A–Y* discharge)] on the VTC curve (path D). Here, the paths Ⓓ and ⓓ designated the changes in the cell voltages for the on- and off-cells caused by the decrease in the ramp set-down voltage, respectively. In this case, a lower set-down voltage level was needed to move the cell voltages to the *X–Y* and *A–Y* simultaneous discharge (or initialization) point. Meanwhile, the wall voltages moved to the lower-left based on a slope of $^1/_2$ when the *X–Y* discharge was produced. In addition, when the *X–Y* and *A–Y* simultaneous discharge occurred, the wall voltages moved to the lower-left based on a slope of 1. The paths ⓓ and ⓓ designated the changes in the wall voltages for both the on- and off-cells due to the reset weak discharge caused by the decrease in the ramp set-down voltage, respectively. The changes in the wall voltages for the on- and off-cells were also measured by the method described in Fig. 5(a) and (c). At the termination of the ramp set-down for both the on- and off-cells, the cell voltages were located at the *X–Y* and *A–Y* simultaneous discharge (or initialization) point, whereas the wall voltages were located at the same point as the initial wall voltage, indicating a successful initialization through the reset process for both the on- and off-cells. In this case, the values of V_B and V_{SD} affected the location of the wall voltages that determined the sustain margin. Moreover, it should be kept in mind that the values of V_B and V_{SD} need to be controlled properly to avoid a misfiring discharge when the negative X-bias, V_Z is applied during an address period.

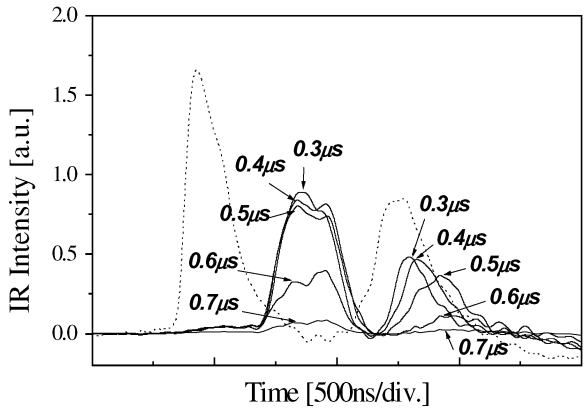

Fig. 7. Changes in IR (828 nm) emission waveforms from undesired discharge between Y_n and A_{n+1} relative to transition time, T_{TR}, during address process, where dotted lines indicate IR emission waveforms during primary and secondary address discharges between Y_n and A_n.

3) Wall-Charge Generation Region in Address-Period (E–F Region in Fig. 3): At point E in Fig. 3, where the scan voltage abruptly increased by V_{SC} and the *X*-bias voltage abruptly decreased by $V_B + V_Z$, the cell voltages moved along path E, whereas the wall voltages did not change, as there was no discharge. In Fig. 6(c), the paths Ⓔ and ⓔ designated the changes in the cell voltage for the on- and off-cells, respectively, when applying the scan voltage and *X*-bias voltage, as shown in point E in Fig. 3. The points Ⓔ and ⓔ designated the wall voltage positions for the on- and off-cells, respectively, which were located unchanged due to the absence of discharge, as shown in Fig. 6(c). For the on-cells, when the negative scan pulse V_{SC} and positive address pulseV_A were simultaneously applied [(F) in Fig. 3], the primary address discharge was produced between the *Y* and *A* electrodes, indicating that the resulting cell voltage for the on-cells exceeded V_{tAY}(Ⅱ) along path Ⓔ in the VTC curve, as shown in Fig. 6(c). Meanwhile, for the off-cells, the

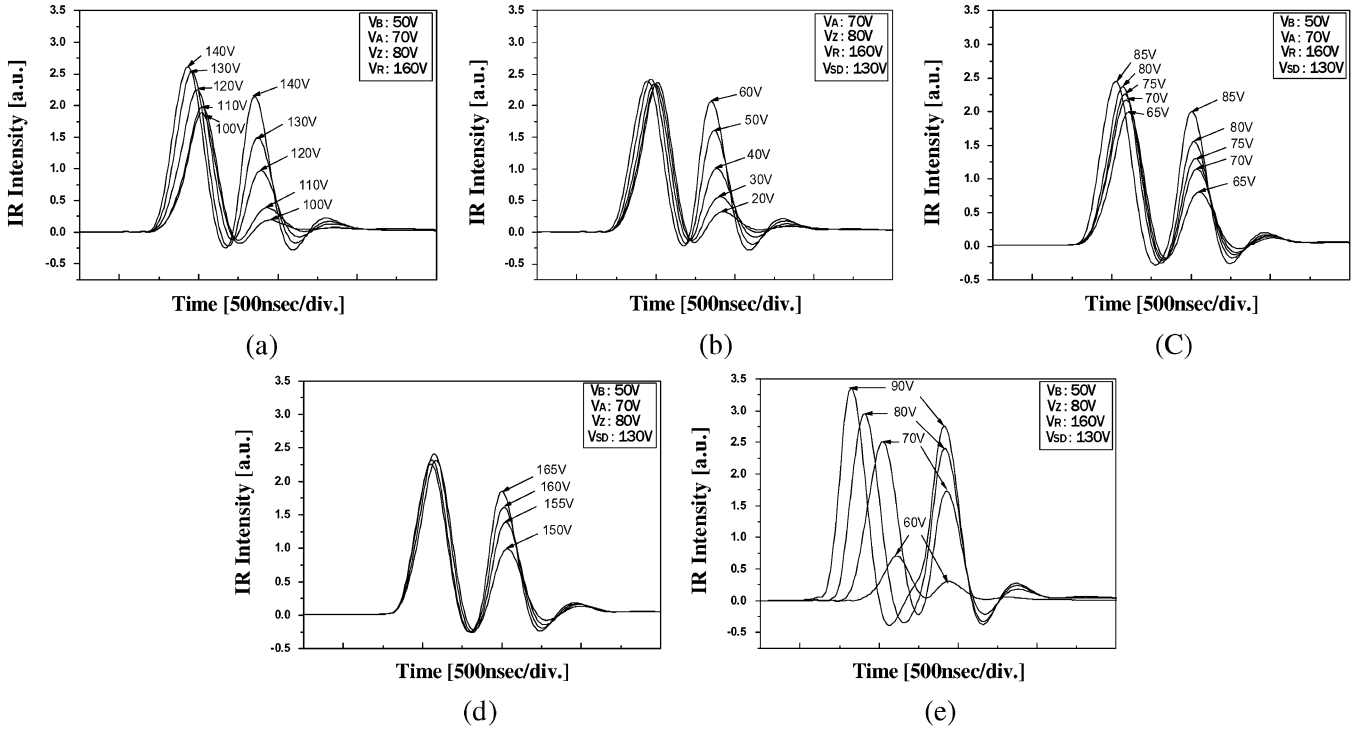

Fig. 8. IR waveforms measured during primary and secondary address discharges with various (a) set-down voltages $V_{\rm SD}$, (b) bias voltages V_B in reset-period, (c) negative bias voltages V_Z, (d) reverse positive scan pulses V_R, and (e) address pulse voltages V_A in address period.

path F did not exceed $V_{\rm tAY}$(II) in the VTC curve, because no address pulse was applied, as shown in Fig. 6(c). Here, the paths E and E designated the changes in the cell voltages for the on- and off-cells, respectively. Since the main function of the primary address discharge in the proposed bipolar scan waveform with a very short address pulsewidth (≤ 1 μs) is only to generate wall charges, the wall charges on the scan and address electrodes almost disappeared during the primary address discharge, so that the wall voltage for the on-cells moved to the lower-left along path f, yet the wall voltage for the off-cells did not move (point F), as shown in Fig. 6(c). Here, the point F designated the position of wall voltage for the off-cells, whereas the path f designated the changes in the wall voltage for the on-cells.

4) Wall-Charge Accumulation Region in Address-Period (G Region in Fig. 3): As shown at point G in Fig. 3, when the reverse positive scan pulse, V_R, was applied immediately after applying the negative scan pulse, the potential difference between $+V_R$ and $-V_Z$ produced another address discharge, i.e., a secondary address discharge, only for the on-cells thanks to the presence of the priming particles generated by the previous primary address discharge. However, for the off-cells, the potential difference between $+V_R$ and $-V_Z$ did not produce a secondary address discharge due to the absence of priming particles. Since the main function of the secondary address discharge is to accumulate wall charges for the subsequent sustain discharge, the width of the reverse positive scan pulse was about 4 μs. This secondary address discharge can be considered as a kind of first sustain discharge produced between the *Y* and *X* electrodes during an address period. The paths G and G designated the changes in the cell voltages for the on- and off-cells, respectively. For the on-cells, the cell voltage exceeded $V_{\rm tYX}$(I) along path G in the VTC curve when applying the reverse positive scan pulse, resulting in a strong *Y–X* discharge. Conversely, for the off-cells, the cell voltage did not exceed $V_{\rm tYX}$(I) along path G in the VTC curve when applying the reverse positive scan pulse, as the wall charge state between the off- and on-cells was different due to the primary address discharge. As a result, prior to the sustain-period, the wall voltages for both the on- and off-cells were located at different points, as shown in Fig. 6(d). The position of wall voltage for the off-cells, g remained unchanged, and were located far away from the discharge start threshold cell voltage between *X* and *Y* [$V_{\rm tXY}$(I)]. On the other hand, the position of wall voltage for the on-cells moved along path g, and were located near the discharge start threshold cell voltage between *X* and *Y* [$V_{\rm tXY}$(I)], where the path g designated the changes in the wall voltage for the on-cells. Thus, in the sustain-period, when the sustain pulse was applied to the *X* electrode, the sustain discharge was only produced for the on-cells due to the different locations of the on- and off-cells, as shown in Fig. 6(d).

III. Experimental Results and Discussions

Fig. 7 shows the measured IR (828 nm) emission waveforms emitted from the undesired discharge between Y_n and A_{n+1} in Fig. 2(c) relative to the transition time $T_{\rm TR}$ during an address process. The dotted lines in Fig. 7 indicate the IR emission waveforms during the primary and secondary address discharges in the previous scan line, i.e., between Y_n and A_n in Fig. 2(c). With a transition time of 0.3 μs, undesired first misfiring discharges were produced, triggered by the overlapped address pulse, plus an undesired secondary address discharge was also produced, thereby turning on undesired cells during

the sustain period. However, increasing the transition time $T_{\rm TR}$ lowered the electric field induced by the abrupt change of the scan pulse from the forward scan voltage $V_{\rm SC}$ to the reverse scan voltage V_R enabling the undesired address discharge to be suppressed, as shown in Fig. 7. When increasing the transition time $T_{\rm TR}$ from 0.3 to 0.6 μs, the undesired first address discharge was weakened, along with the second. In the case of a transition time $T_{\rm TR}$, over 0.7 μs, the undesired misfiring problem was completely removed. Thus, with a transition time $T_{\rm TR}$, over 0.7 μs, the five parameters of $V_{\rm SD}, V_B, V_Z, V_R$, and V_A were carefully examined: the scan ramp set-down voltage $V_{\rm SD}(<0)$ varied from -100 to -140 V, the positive *X*-bias voltage $V_B(>0)$ ranged from 20 to 60 V during the set-down period, the negative *X*-bias voltage $V_Z(<0)$ varied from -65 to -85 V during the address period, and the reverse positive scan pulse, V_R, ranged from 150 to 165 V and the address pulse, V_A, ranged from 60 to 90 V. The total time for the reset- and address periods was 390 and 480 μs, respectively. The amplitude of the sustain pulse was 160 V and the operating frequency was 100 kHz.

Fig. 8 shows the changes in the IR waveforms measured during the primary and secondary address discharges when varying the above five parameters. The IR emission data in Fig. 8(a) indicate that both the primary and secondary address discharge intensities depended strongly on the set-down voltage $V_{\rm SD}$ in the reset-period. When $V_{\rm SD}$ increased, the primary and secondary address discharges both intensified. As mentioned above, a lower voltage level for $V_{\rm SD}$ is necessary in the reset-period in order to move the cell voltages to the simultaneous initialization point in the VTC curve. Fig. 8(b) shows that the positive *X*-bias voltage V_B during the set-down period only affected the secondary address discharge. As shown in Fig. 8(b), when V_B increased, the secondary address discharge intensity also increased. Yet, the application of the positive *X*-bias voltage, V_B, contributed to erasing the positive wall charges on the *X*-electrode, thereby facilitating the secondary address discharge due to the reduced amount of positive wall charges at the application of $-V_Z$. However, too high a positive *X*-bias voltage, for example, above $+60$ V, caused a misfiring discharge between the *X* and *A* electrodes, because the high voltage of V_B+V_Z caused the cell voltages to exceed $V_{\rm tAX}(\rm III)$, as shown by path E in Fig. 6(c). Accordingly, the positive *X*-bias voltage, V_B, during the set-down period needs to be properly controlled to enhance the secondary address discharge without a misfiring discharge. Fig. 8(c) shows that the negative *X*-bias voltage V_Z during the address period affected both the primary and secondary address discharge. However, too high a negative *X*-bias voltage, such as -85 V, caused a misfiring discharge between the *X* and *A* electrodes, because the high voltage of V_B+V_Z caused the cell voltages to exceed $V_{\rm tAX}(\rm III)$, as shown by path E in Fig. 6(c). As shown in Fig. 8(d), the secondary address discharge intensified with an increase in the reverse positive scan pulse V_R. Meanwhile, in Fig. 8(e), an increase in the address pulse V_A, intensified the primary address discharge, plus the secondary address discharge was also intensified due to the presence of a large amount of priming particles induced by the preceding primary address discharge.

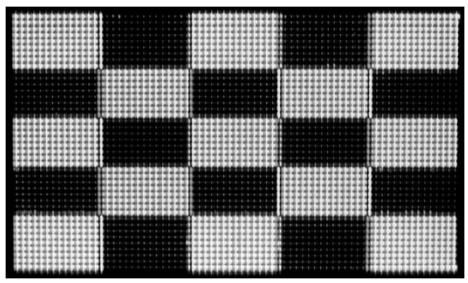

Fig. 9. Checkered pattern consisting of 5×5 squares to check misfiring discharge between adjacent cells in case of adopting proposed high-speed driving waveforms in Fig. 1(b).

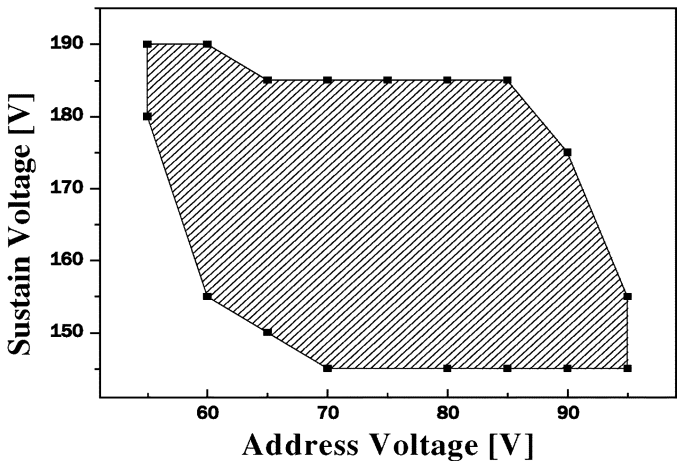

Fig. 10. Dynamic voltage margin with checkered pattern in Fig. 9 when adopting proposed high-speed driving waveforms in Fig. 1(b).

Fig. 9 shows a checkered pattern displaying white and black images alternately and consisting of 5×5 squares in the case of using the proposed driving waveforms in Fig. 1(b) with optimized voltage levels. As shown in Fig. 9, the proposed high-speed driving waveforms successfully displayed the checkered pattern under an address pulsewidth of 1 μs at an address voltage of 60 V. Fig. 10 shows the dynamic voltage margin measured when displaying the checkered pattern using the proposed high-speed driving waveforms on the 4-in test panel. As shown in Fig. 10, when optimizing the various voltage levels in the proposed high-speed driving waveforms, good dynamic voltage margin characteristics were obtained.

IV. Conclusion

This paper proposed a high-speed driving method using the bipolar scan waveform with a scan width of 1 μs. A misfiring discharge is avoided during the overlap by increasing the transition time from the forward to the reverse scan pulse to over 0.7 μs. Based on a V_t close curve analysis, the voltage levels for the bipolar scan pulse and related parameters, such as $V_{\rm SD}, V_B$, and V_Z, were optimized, and their validity tested using a checkered pattern on a 4-in test panel. As a result, a high-speed address with a scan width of 1 μs was successfully obtained at an address voltage of less than 60 V.

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