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Effects of Address-on-Time on Wall Voltage Variation during Address-Period in AC Plasma Display Panel*

Byung-Tae CHOI[†], **Hyung Dal PARK**[†], *Nonmembers*, *and* **Heung-Sik TAE**[†a)], *Member*

SUMMARY To explain the variation of the address discharge during an address period, the wall voltage variation during an address period was investigated as a function of the address-on-time by using the V_t closed curves. It was observed that the wall voltage between the scan and address electrodes was decreased with an increase in the address-on-time. It was also observed that the wall voltage variation during an address period strongly depended on the voltage difference between the scan and address electrodes. Based on this result, the modified driving waveform to raise the level of V_{scanw}, was proposed to minimize the voltage difference between the scan and address electrodes. However, the modified driving waveform resulted in the increase in the falling time of scan pulse. Finally, the overlapped double scan waveform was proposed to reduce a falling time of scan pulse under the raised voltage level of V_{scanw}, also.

key words: *wall voltage variation during address-period, address-on-time, V_t closed curves, voltage difference between scan and address electrodes, overlapped double scan pulse*

1. Introduction

For the realization of the full high-definition plasma display panels (full-HD PDPs), the high-speed address has become one of the most important issues, especially under the address-display-separated (ADS) driving method [1]–[9]. The full color images are displayed as a result of superposition of the on- and off-cell states during one TV-field. Thus, the successful display of various images strongly depends on how uniformly the wall charges on three electrodes maintain throughout the address-period. However, as the cell size decreases, the corresponding scanning time becomes much longer due to the increase in the scan line under the current ADS driving scheme. Accordingly, the high-speed single scan technique has become a very critical issue to be realized urgently, especially for the successful realization of the full-HD PDPs with 1080 scan lines. The address delay is determined by the sum of address discharge delay and the falling time of scan pulse. The address discharge delay, especially the discharge delay determined by the formative time lag, strongly depends on the electric field intensity induced by the sum of the wall voltage and the applied voltage. For address discharge delay, the maintenance of the constant wall voltage within the cells throughout the address-period is very important factor for the high-speed address. On the other hand, for the delay related to the falling time of scan pulse, the driving waveform to shorten the falling time of scan pulse is required. Our experiment result shows that the aggravated address discharge condition especially during the latter part of the address-period is deeply related to the address-on-time which is determined by the number of the applied address pulse [10]. In the mean time, the address discharge delay in a cell is also affected by the priming particles in the adjacent cells [11]. Since the priming particles provided in the adjacent cells mainly affects the statistical time lag, the effects of priming particles are neglected in this study. When the address discharge delays were measured, the adjacent cells were maintained to be 'off-state' to eliminate completely the priming effect in this study.

In this paper, the wall voltage variation during an address-period was investigated as a function of the address-on-time using the V_t closed-curve analysis [4], [9], [12], [13]. In particular, the wall voltage variations due to different voltages applied to the Y electrode during an address-period, were examined. Based on the analysis on the wall voltage variation during the address-period, the voltage levels in V_{scanw}, were varied to minimize the wall voltage variation irrespective of the increase in the address-on-time during the address-period. In order to shorten the falling time of scan pulse without misfiring discharge, the overlapped double scan waveform was proposed.

2. Experimental Set-Up

The 6-in. ac PDP filled with a Ne-Xe (11%) gas mixture at 450 Torr was used as a test panel. The test panel had a conventional ac-PDP structure with square-type closed barrier ribs and three electrodes such as two sustain and one address electrodes. The cell pitch of the test panel was the same as that of the 42-in. HD grade PDP. The specifications of the 6-in. test panel are given in Table 1.

Table 1 Specifications of 6-in. test ac-PDP used in this study.

Front Panel		Rear Panel	
ITO width	200 μm	Barrier rib width	50 μm
ITO gap	77 μm	Barrier rib height	120 μm
Bus width	65 μm	Address width	90 μm
Cell pitch		912 μm × 693 μm	
Gas chemistry		Ne-Xe (11 %)-He (35 %)	
Barrier rib type		Closed rib	

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[†]The authors are with School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu 702-701, Korea.

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a) E-mail: hstae@ee.knu.ac.kr

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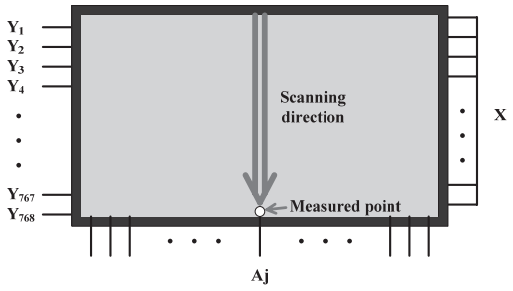

Fig. 1 HD grade PDP with three electrodes where X is common (sustain) electrode, Y is scan electrode separated from Y_1 to Y_{768}, and A is address electrode. Arrow seen above indicates scanning direction, and measured cell is located at last ($=Y_{768}$) scan linen and at A_jth addresses line.

Figure 1 shows the schematic diagram of the typical HD grade PDP with 768 scan lines where X is a common electrode, Y is a scan electrode separated from Y_1 to Y_{768}, and A is an address electrode. As shown in Fig. 1, after the reset-procedure on the entire region of the PDP, the line-by-line scanning was carried out sequentially from the first scan line, Y_1 to the last, Y_{768} during the address-period. In this experiment, to have the same effect as the address discharge produced at the A_jth cell of the last ($=Y_{768}$) scan line in Fig. 1, the address discharge in the 6-in. test panel was measured at 921.6 μs (=1.2 μs $\times$ 768 scan lines) after the reset period. In this case, the non-uniform distribution of priming particles can not affect the address discharge characteristics because the address discharge was measured at 921.6 μs after the reset period [14]. The address electrode of the A_jth cell of the last (= Y_{768}) scan line experiences the different voltage variations depending on whether the address discharge has been produced in the prior cells located on the A_jth address electrode.

Figure 2 shows the five test patterns for examining the effects of the address-on-time on the wall voltage variations at the A_jth cell located at the last ($=Y_{768}$) line. The measurement A_jth cell located at the 768th line in Fig. 2 means the cell measured at 921.6 μs (=1.2 μs $\times$ 768 scan lines) after the reset period in the 6-in. test panel. Figure 3 shows the driving waveforms employed to display the five test patterns of Fig. 2. In the driving waveforms of Fig. 3, the voltages applied to the X and Y electrodes were all the same for the five test patterns of Fig. 2 except the address pulses applied to the A_jth electrode. In this experiment, the address discharges were measured only at the A_jth cell located at the last ($=Y_{768}$) line to analyze the wall voltage variation depending on the various display patterns. Case 1 in Fig. 2 was a full black-pattern, indicating that there was no address discharge from the 1st to 768th line except the last line. Accordingly, the address-on-time in case 1 was zero. As shown in case 1 of Fig. 3, the address pulse was applied only to the 768th line. Case 2 (i) of Fig. 2 was a half white-pattern with continuous address discharges from the 100th to 483rd line. As shown in case 2 (i) of Fig. 3, the 384 address pulses were applied continuously only from the 100th to 483rd line. Case 2 (ii) in Fig. 2 was a half white-pattern with discrete address discharges. The address discharges were produced alternately, so that the 10 address discharge-on and -off transitions were made from the 1st to 767th line. This meant that the 10 voltage variations from 0 to 60 V or 60 to 0 V occurred at the address electrode of the A_jth cell. Case 2 (iii) in Fig. 2 was also a half white-pattern with discrete address discharge. Like case 2 (ii), the

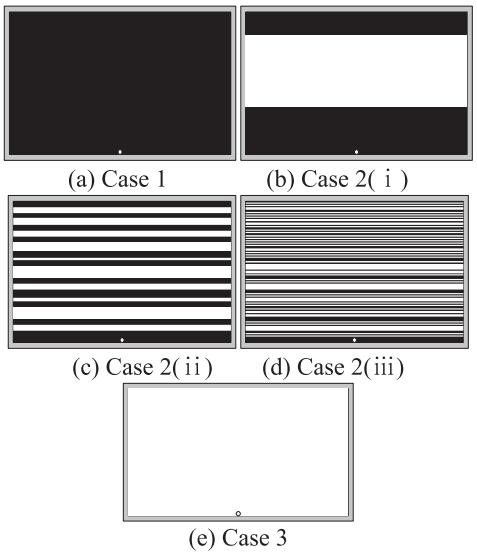

Fig. 2 Five test patterns for examining wall voltage variation in cells between first ($=Y_1$) and last ($=Y_{768}$) line where (a) is full black, (b) is half white with continuous address discharges from 100th to 483rd line, (c) is half white with discrete address discharges, that is, number of transition from address discharge-on into address discharge-off states from 1st to 767th line is 10, (d) is half white, that is, number of transition from address discharge-on into address discharge-off states from 1st to 767th line is 40, and (e) full white.

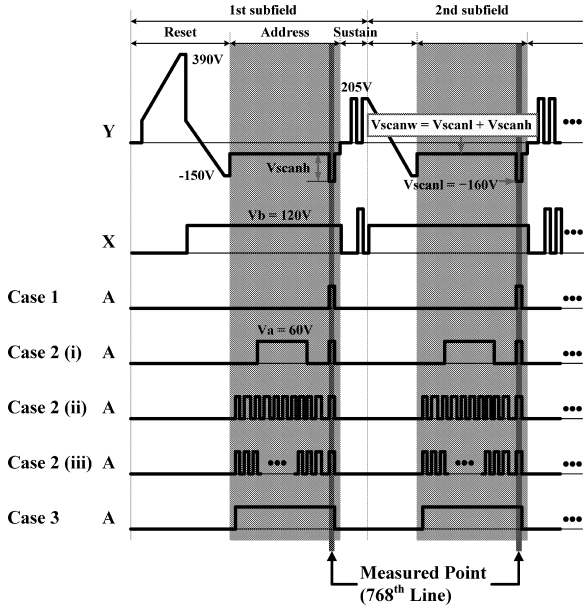

Fig. 3 Driving waveforms employed to display five test patterns of Fig. 2.

address discharges were produced alternately, but the 40 address discharge-on and -off transitions were made from the 1st to 767th line. This meant that the 40 voltage variations from 0 to 60 V or 60 to 0 V occurred at the address electrode of the A_jth cell, even though the 384 address pulses were applied to display the full-white-pattern of case 2 (iii) in Fig. 2. For cases 2 (i), (ii), and (iii), the address-on times were exactly the same, namely, 460.8 μs (=1.2 μs × 384 scan lines). The case 3 in Fig. 2 was a full white-pattern. The address-on time for case 3 was 921.6 μs (= 1.2 μs × 767 scan lines). As shown in case 3 of Fig. 3, the 767 address pulses were applied continuously from the 1st to 767th lines. In this experiment, the address discharge time per a line was 1.2 μs, so that the total address discharge time for the 768 scan lines was 921.6 μs (=1.2 μs × 768). As shown in Fig. 3, during an address-period, for the on-cells, the scan low voltage, V_{scanl} of the negative-going scan pulse applied to the Y electrode was fixed at −160 V, whereas, for the off-cells, the scan voltage, V_{scanw} (=V_{scanl} + V_{scanh}) was varied from −100 to +40 V. The address voltage, V_a was fixed at 60 V.

3. Results and Discussion

3.1 Effects of Address-on-Time on Wall Voltage Variations during Address-Period

Figures 4(a) and (b) shows the IR (=828 nm) waveforms emitted during the address discharge and the corresponding address delay times measured at the A_jth cell located in the last 768th scan line from the test panel when adopting the five different test patterns shown in Fig. 2. In case 1, the fast address discharge initiation with high IR peak was observed, whereas in case 3, the slow address-discharge initiation with low IR peak was observed. As shown in Fig. 4, the application of address pulses prior to the last 768th scan line induced the retardation of address discharge initiation. However, in cases 2 (i), (ii), and (iii), the address discharge initiation remained almost constant irrespective of the number of the voltage variation from 0 to 60 V and 60 to 0 V. Accordingly, it is confirmed that the retardation of the address discharge initiation strongly depends on not the number of the address voltage variation but the number of the application of the address pulses (i.e., an address- on-time).

Figure 5 shows the changes in the V_t closed curves measured for both cases 1 and 3, i.e., full-black test pattern (case 1) and full-white test pattern (case 3) with respect to the wall voltage state after the reset-period in the 767th line prior to the last address discharge. The reference in Fig. 5 means zero wall voltage condition. In Fig. 5, the full-black test pattern (case 1) showed no change in the V_t closed curves between the 1st and the 767th scan line, meaning that there was almost no wall- charge variation in the full-black test pattern throughout the address-period. However, as shown in the first quadrant of the V_t closed curves in the full-white test pattern (case 3) of Fig. 5, the firing threshold voltage between the *Y-A* electrodes was moved to the upward direction by about 15 V, and the firing threshold voltage between the *X-Y* electrodes was moved to the right direction by about 5 V with respect to the wall voltage state prior to the address period (i.e., after reset). The voltage variations of 15 V and 5 V mean the reduced wall voltages between the *Y-A* electrodes and between the *X-Y* electrodes, respectively. Since the electric field intensity induced by the sum of the wall voltage and the applied voltage affect the address discharge delay, the reduction of wall voltage means a delay of the address discharge under the constant applied voltage conditions. Accordingly, this wall voltage reduction resulted in a delay of the address discharge, as shown in Fig. 4. Meanwhile, the V_t closed curves for the reference and after-reset indicated that through the reset discharge, the negative wall charges were accumulated on the X and Y electrodes whereas the positive wall charges were accumulated on the A electrode.

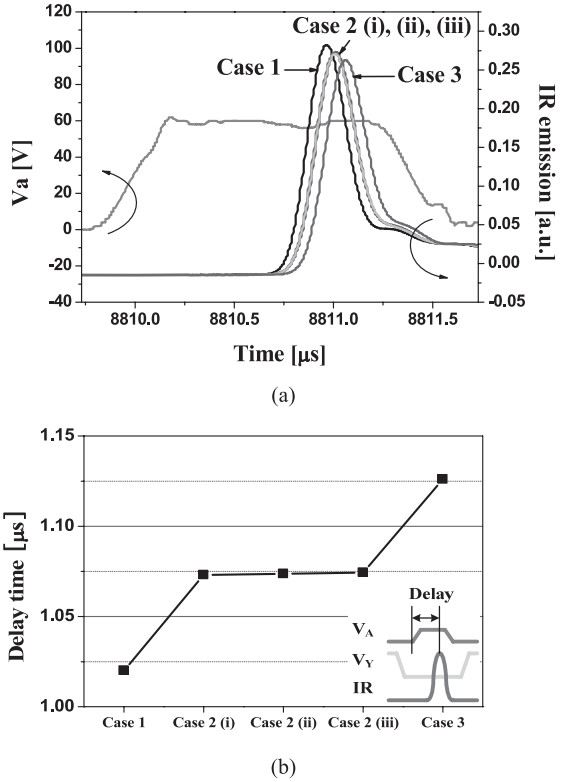

Fig. 4 (a) IR waveforms emitted during address discharge at A_jth cell in 768th line relative to cases 1, 2 (i), (ii), (iii), and 3 in Fig. 2, and (b) corresponding address delay times.

Figures 6(a) and (b) show the voltage difference among the three electrodes X, Y, and A experienced at the measurement cell (A_jth cell in 768th line) during the line-by-line scanning from 1st to 767th line when displaying the two different display patterns such as (a) full-black pattern (case 1) and (b) full-white pattern (case 3). For cases 1 and 3, the voltages applied to both the X and Y electrodes for 927.67 μs (= 1.2 μs × 767 scan lines) were +120 V (=V_b in Fig. 3) and −80 V (=V_{scanw} in Fig. 3), respectively. On the other hand, the voltages applied to the A electrode for 927.67 μs were 0 V for the full-black pattern (case 1), and 60 V for the full-

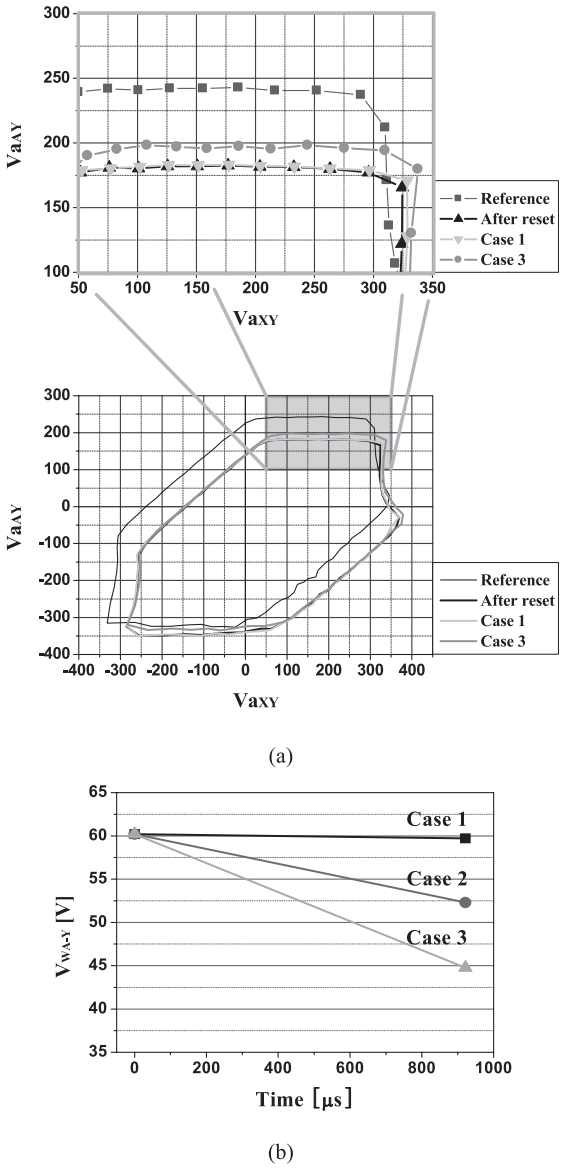

Fig. 5 (a) V_t closed curves measured for full-black (case 1) and full-white (case 3) test patterns with respective to wall voltage state after rest-period where reference means zero wall voltage condition, and (b) variations in wall voltages between A-Y electrodes during address period for three cases 1, 2, and 3.

white pattern (case 3). Accordingly, for the full-white pattern, the large voltage difference (= 140 V) between the A-Y electrodes has been applied for 927.67 μs, implying that the full- white pattern (case 3) induces the larger voltage difference between the A-Y electrodes, thus resulting in a decrease in the wall voltage necessary for the fast address discharge at the 768th line.

3.2 Effects of Voltage Level Applied to Scan-Electrode (= V_{scanw}) on Wall Voltage Variations during Address-Period

Figure 7 shows the changes in the address delay time relative to the voltage level of V_{scanw} (=V_{scanl} + V_{scanh}) so as to measure the effect of the voltage difference between the A-Y electrode on the delay time during an address period. In Fig. 7, V_{scanw} was varied from −95 to +40 V by varying the V_{scanh} from 65 to 200 V during an address-period. The address delay in Fig. 7 has two slopes when varying the V_{scanw} from −95 V to 40 V. The negative slope in the address delay of Fig. 7 means a reduction of address discharge delay, which is mainly caused by the minimization of wall voltage variation in cases 2 and 3. The positive slope in the address delay of Fig. 7 means an increase in the address delay, which is mainly caused by the increase in the falling time of scan pulse in all cases 1, 2, and 3. The decrease in the wall voltage during an address-period could be unavoidable because the wall charge loss was induced by the potential difference applied between the A-Y electrodes throughout the address-period. This meant that the wall charge loss was increased that with an increase in the potential difference between the A-Y electrodes. Accordingly, the efficient way to minimize the wall charge variation throughout the address period was to minimize the potential difference between the A-Y electrodes by raising the voltage level of V_{scanw} higher. However, as the voltage level of V_{scanw} is higher, the falling time from V_{scanw} to V_{scanl} was increased, thereby causing the address delay time to be longer.

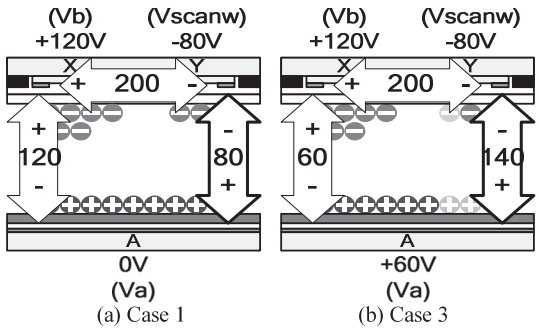

Fig. 6 Voltage differences among three electrodes X, Y, and A experienced at A_jth cell in 768th scan line during line-by-line scanning from 1st to 767th line in address-period for two test patterns: (a) full-black test pattern (case 1), and (b) full-white test pattern (case 3).

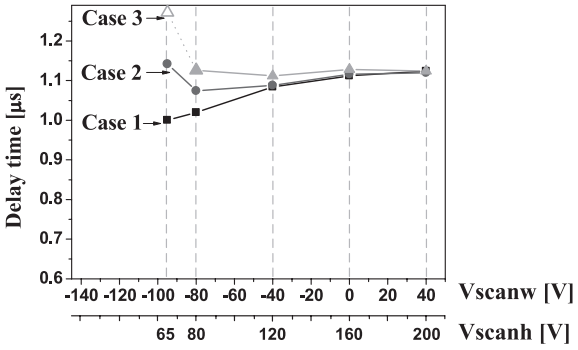

Fig. 7 Changes in address delay time relative to variation of V_{scanw} (=V_{scanl} + V_{scanh}) for different address-on-times (cases 1, 2, and 3).

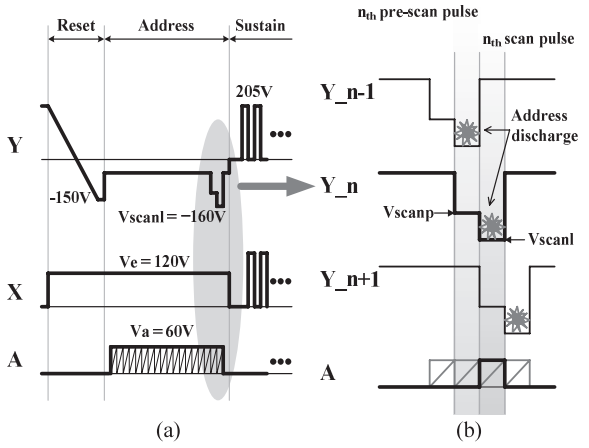

Fig. 8 (a) Driving waveform with proposed double scan pulse consisting of pre-scan and scan pulses, and (b) enlarged double scan pulse applied from $(n-1)$th to $(n+1)$th scan line.

3.3 Overlapped Double-Scan Pulse for Minimizing Wall-Voltage Variation During Address-Period

To minimize the address delay due to a falling time of the scan pulse in case of raising the voltage level of V_{scanw}, the double scan pulse is proposed, as shown in Fig. 8. The falling time is defined as a time taken in varying the voltage level from V_{scanw} to V_{scanl}. The falling time of the single scan pulse was about 500 ns at V_{scanh} of 160 V in this study. The double scan pulse consists of a pre-scan pulse with a higher voltage level and scan pulse with a lower voltage level. In the double scan pulse, the pre-scan pulse can be overlapped with the pervious scan pulse if the voltage level of the pre-scan pulse ($=V_{scanp}$) is higher enough to prevent misfiring. Accordingly, under this condition, the pre-scan pulse is applied simultaneously at the nth line at the application of the $(n-1)$th scan pulse. The resultant falling time of the proposed double scan pulse is expected to be much shorter than that of the conventional scan pulse with a raised voltage level of V_{scanw}. At V_{scanp} of −120 V, the falling time from V_{scanp} to V_{scanl} was about 300 ns. As shown in the IR emissions of Fig. 9, the voltage level of the pre-scan pulse, V_{scanp}, was be chosen on condition that no address discharge was produced during nth scan pulse even at the application of the address pulse during the nth pre-scan pulse. As a result, the lowest value of V_{scanp} for preventing the misfiring discharge was −127 V in this study.

Figure 10 shows the changes in the address delay when adopting the proposed double scan pulse during an address-period. The address delay time was decreased even though the voltage level of V_{scanw} was increased. For the conventional scan pulse, the address delay was observed to be 1.12 μs at V_{scanw} of 40 V (V_{scanh} = 200 V) for all cases 1, 2, and 3. On the other hand, for the proposed double scan pulse, the address delay was reduced from 1.12 to 0.9 μs at V_{scanw} of 40 V (V_{scanp} = −120 V and V_{scanl} = −160 V) for all cases 1, 2, and 3.

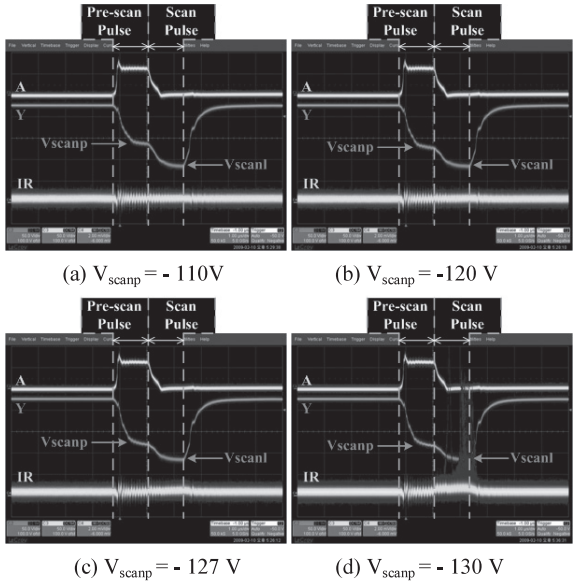

Fig. 9 IR waveforms relative to V_{scanp} level during application of address pulse.

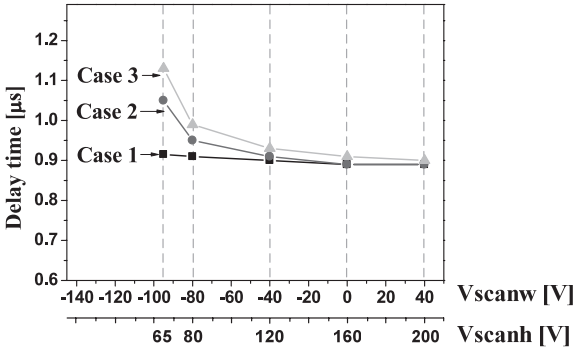

Fig. 10 Delay time relative to cases of previous discharge time on address electrode when double scan pulse applied.

4. Conclusions

The realization of a uniform address discharge throughout an address-period is an important factor for a high speed address. In this study, it was observed that the variation of the address discharge resulted from the wall voltage variation during the address period. The V_t closed curves analysis confirmed that the two factors inducing the wall voltage variation during an address-period are the number of the applied address pulse (i.e., address-on-time) and the voltage difference between the scan and address electrodes. The decrease in the wall voltage during an address-period seems unavoidable because the wall charge loss is induced by the potential difference applied between the scan and address electrodes throughout the address-period. This meant that as the potential difference between the scan and address electrodes was increased, the wall charge loss was increased. Accordingly, it was found that the efficient way to minimize the wall charge loss throughout the address-period was to

minimize the potential difference between the scan and address electrodes by raising the voltage level of V_{scanw} higher. As a result, under the raised voltage level of V_{scanw}, the double scan pulse that could reduce the falling time of scan pulse was proposed to reduce the address delay by minimizing the wall voltage variation irrespective of the address-on-time.

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Byung-Tae Choi received a B.S., and M.S. degrees in electronic and electrical engineering from Kyungpook National University, Daegu, Korea, in 2004, and 2006, respectively. He is currently pursuing the Ph.D. degree in electronic engineering at the same university. His current research interests include plasma physics, microplasma and driving method of plasma display panels (PDPs).

Hyung Dal Park received the M.S. degrees in electronic and electrical engineering from Kyungpook National University, Daegu, Korea, in 2007. He is currently pursuing the Ph.D. degree in electronic engineering at the same university. His current research interests include plasma physics, application of microplasma, and driving of dielectric-barrier discharge (DBD).

Heung-Sik Tae received a B.S., M.S., and Ph.D. degrees in electrical engineering from the Seoul National University, Korea, in 1986, 1988, and 1994, respectively. Since 1995, he has been a Professor in the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, Korea. His research interests include the optical characterization and driving waveform of plasma display panels (PDPs), the design of millimeter wave guiding structures, and electromagnetic wave propagation using meta-material. Dr. Tae is a member of the Society for Information Display (SID). He has been serving as an Editor for the IEEE Transactions on Electron Devices section on display technology since 2005.