LETTER

Dual-Slope Ramp Reset Waveform to Improve Dark Room Contrast Ratio in AC PDPs*

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SUMMARY A new dual-slope ramp (DSR) reset waveform is proposed to improve the dark room contrast ratio in AC-PDPs. The proposed reset waveform has two different voltage slopes during a ramp-up period. The first voltage slope lower than the conventional ramp voltage slope plays a role in producing the priming particles under the low background luminance, which is considered to be a kind of pre-reset discharge. On the other hand, the second voltage slope higher than the conventional ramp voltage slope produces a stable reset discharge due to the presence of the priming particles, but gives rise to a slight increase in the background luminance. Thus, a bias voltage is also applied during a part of the second voltage-slope period to adjust the background luminance and address discharge characteristics. As a result, the proposed dual-slope reset waveform can lower the background luminance without causing the discharge instability, thereby improving the high dark room contrast ratio of an AC-PDP without reducing the address voltage margin.

key words: *plasma display panel, dual-slope ramp reset waveform, dark room contrast ratio, background luminance*

1. Introduction

Plasma television (TV) is believed to be a promising candidate for large area (> 40 inch), self-emitting, digital high definition home theater TVs. Therefore, improving the image quality generated by a plasma TV is a critical issue for current PDP technology. In particular, improving the dark room contrast ratio is a very important factor contributing to the high image quality required for a plasma home theater TV. As a result, a lot of research has focused on reducing the background luminance during a reset period [1]–[7]. The voltage slope during a ramp-up period also has a considerable affect on the background luminance as well as the address discharge characteristics. However, improving the dark room contrast ratio by controlling the voltage slope during a ramp-up period is difficult, since the conventional ramp reset waveform only has one voltage slope during a ramp-up period. As Sakita [8] has said, the slow up-going ramp waveform induces a very weak discharge stably under the low background luminance, but it takes a long time to accumulate lots of wall charges for the subsequently stable address discharge. On the other hand, if the slope of the up-going ramp waveform goes steeper to reduce the reset time, the reset discharge tends to be a strong discharge instead of a weak discharge, especially without the presence of the priming particles, thereby resulting in increasing the background luminance. The previous research on the reset waveform has often neglected the importance of the priming particles in the reset discharge, that is, the effects of a kind of pre-reset discharge on the reset discharge characteristics. Accordingly, this letter proposes a new dual-slope ramp (DSR) reset waveform to improve the dark room contrast ratio in AC-PDPs, where the proposed reset waveform has two different voltage slopes during a ramp-up period. The reset discharge during the first slow voltage slope ramp-period provides the priming particles under the low background with the subsequent reset discharge during the second fast voltage slope ramp-period. In addition, a bias voltage is also applied during a part of the second voltage-slope period to adjust the background luminance and address discharge characteristics.

2. Experimental Setup

A typical 7-in. ac-PDP was used as the test panel with a conventional three-electrode coplanar structure, as shown in Fig. 1. Detailed specifications of the test panel are listed in Table 1. Figures 2(a) and (b) show the driving waveforms employed in the current study, including (a) the conventional ramp reset and (b) proposed DSR reset waveforms. As shown in Fig. 2, the proposed reset waveform has a dual voltage slope instead of one voltage slope during a ramp-up period. The first voltage slope of the DSR waveform is lower than that of the conventional reset waveform, whereas the second voltage slope of the DSR waveform is higher. Furthermore, a bias voltage is applied to the sustain (X) for suppressing the intense surface discharge, especially during a part of the second voltage-slope period, whereas the ad-

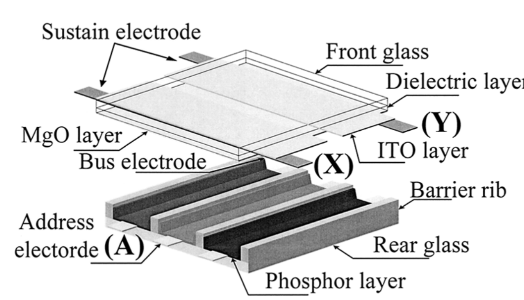

Fig. 1 Schematic diagram of single pixel structure of 7-in. test panel.

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Table 1 Specifications of 7-in. test panel employed in this study.

ITO Width	310 μm
ITO Gap	60 μm
Bus Electrode Width	100 μm
Address Electrode Width	100 μm
Barrier Rib Width	80 μm
Barrier Rib Height	125 μm
Cell Pitch	360 μm
Gas Composition	Ne + Xe (4%)
Gal Pressure	400 Torr
Bus Lines	42

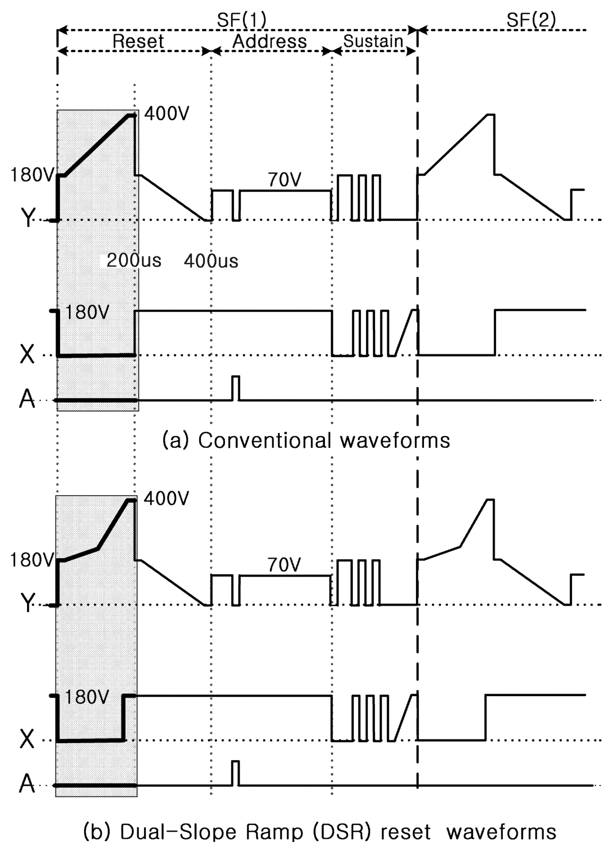

Fig. 2 Driving waveforms employed in current study, including (a) conventional reset and (b) proposed dual-slope ramp (DSR) reset waveforms.

dress (A) electrode remains grounded during a reset-period. To compare the reset discharge characteristics of both the conventional and proposed reset waveforms, the IR emissions were observed using a highly sensitive light detector (Hamamatsu, C6386). Plus, to compare the effects of both reset waveforms on the address discharge characteristics, the dynamic voltage margins were also measured.

3. Results and Discussion

Figure 3 shows the changes in the IR (828 nm) emission waveforms in the case of applying the conventional (I) and proposed DSR (II) reset waveforms at a zero X-bias voltage during a ramp-up period. As shown in Fig. 3, with a zero bias voltage at the X electrode, the first voltage slope

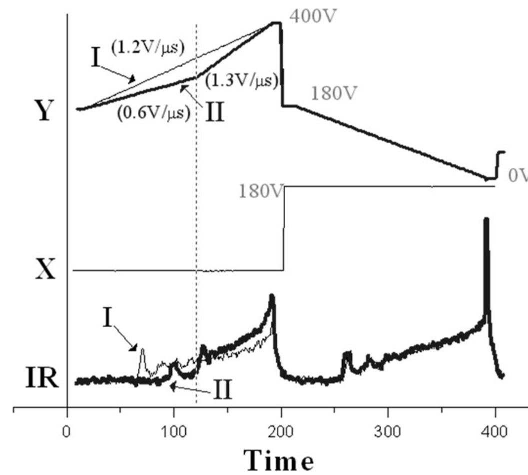

Fig. 3 Changes in IR emission waveforms when applying conventional (I) and proposed DSR (II) reset waveforms.

(=0.6 V/μs) was lower than the conventional ramp voltage slope voltage slope (=1.2 V/μs), thereby reducing the background luminance. Furthermore, the IR emission waveform measured during the first slow voltage-slope period in Fig. 3 indicated that the priming particles were produced under the low background luminance. On the other hand, the second fast voltage slope (=1.3 V/μs) was higher than the conventional ramp voltage slope produced the reset discharge stably even at a fast voltage slope condition, but increased the background luminance.

Thus, to reduce the background luminance during the second voltage slope-period, the increase in the voltage rate between the X and Y electrodes needs to be minimized by applying an X-bias voltage. Since the application time and amplitude of the X-bias voltage can affect both the background luminance and the address discharge characteristics, the biasing condition of the X-bias voltage must be determined very carefully. Figure 4(a) shows the X-bias voltage applied during the second voltage slope-period of the DSR ramp waveform, where ΔT is defined as an time interval between the rising edge of the X-bias voltage and the falling edge of the reset voltage. The time ΔT representing the application time of the X-bias voltage is a very important parameter for both the background luminance and the address discharge characteristics. Figure 4(b) shows the relation between the background luminance and the minimum address voltage with respect to ΔT [3] in the case of applying the proposed DSR reset waveform with a first slow voltage slope of 0.7 V/μs, and a second fast voltage slope of 1.9 V/μs. Unlike the results in Fig. 3, with an X-bias condition of ΔT=30 μs, As shown in Fig. 4(b), when increasing ΔT, the background luminance was decreased, yet the minimum address voltage was increased. In particular, when the ΔT was 50 μs, that is, when the X-bias voltage was applied throughout the second fast up-going ramp period, the reset discharge became very unstable and the misfiring discharge was produced in the ensuing sustain discharge. Accordingly, the optimal condition between the two voltage slopes and

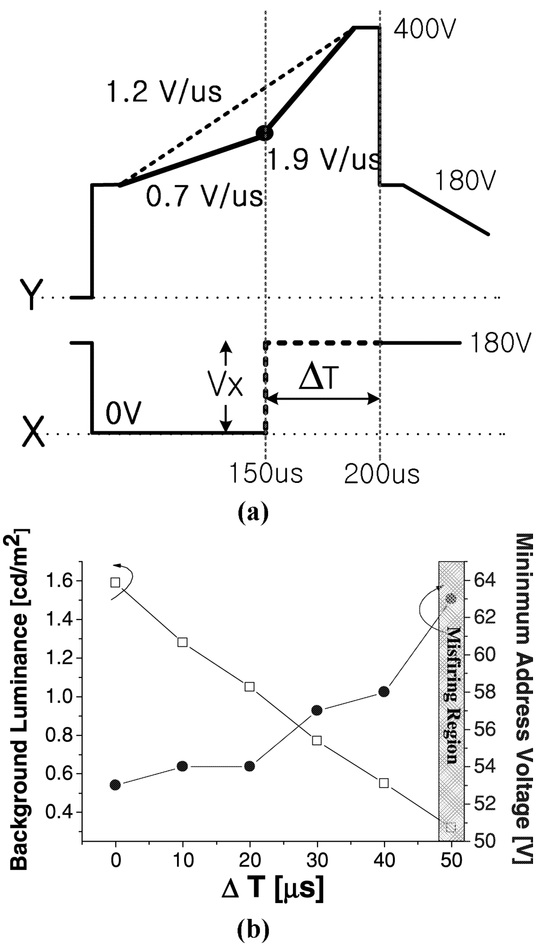

Fig. 4 (a) X-bias voltage applied during second voltage-slope period, where ΔT means application time of X-bias voltage, (b) changes in IR emission waveforms when applying conventional and DSR reset waveform with X-bias of ΔT = 30 μs, and (c) changes in background luminance and minimum address voltage with respect to ΔT.

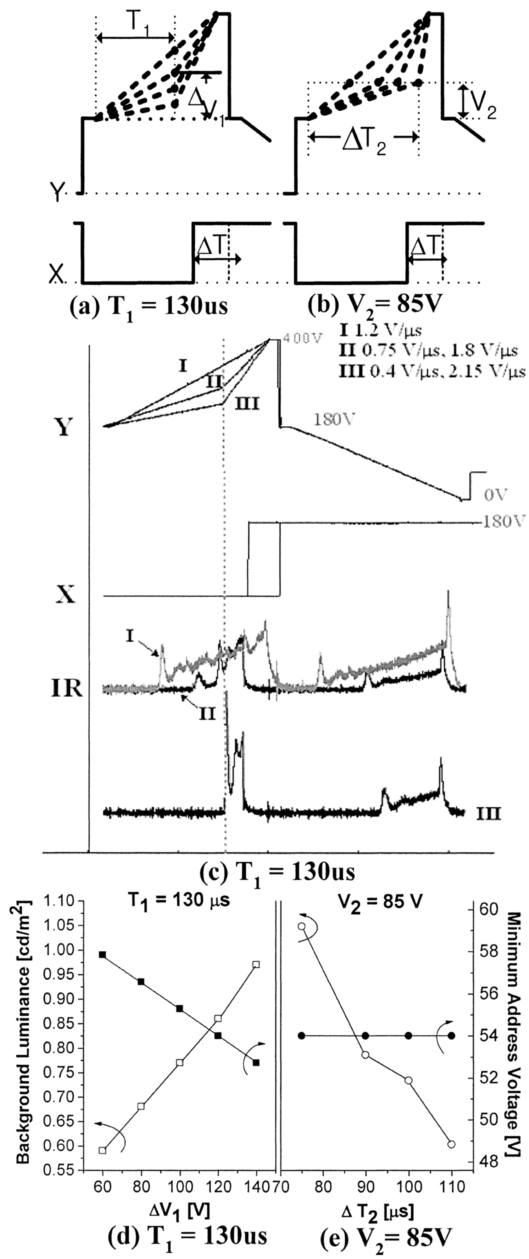

Fig. 5 Changes in background and minimum address voltage [(c) and (d)] for case 1 (a), where first voltage-slope period is fixed at T_1 = 130 μs, and case 2 (b), where amplitude of first voltage-slope-period is fixed at V_2 = 85 V.

the X-bias condition needs to be determined.

Figures 5(a), (b), (c), (d), and (e) show the changes in the IR (828 nm) waveforms (c), the background and minimum address voltage [(d) and (e)] for case 1 (a), where the first voltage-slope period is fixed at ΔT_1 = 130 μs, and case 2 (b), where the amplitude of the first voltage slope-period is fixed at V_2 = 85 V under constant X-bias conditions (i.e., ΔT = 28 μs, Vx = 180 V). In case 1, the amplitude during the first voltage-slope period, i.e. V_1, varied from 60 to 140 V at intervals of 20 V, whereas in case 2, the time interval during the first voltage-slope period, i.e. ΔT_2, varied from 75 to 110 μs. As shown in (II) of case 1 in Fig. 5(c), the IR emissions was decreased when applying the first slow (0.75 < 1.2 V/μs) voltage slope ramp waveform, implying that the priming particles were produced under the low background luminance during the first slow up-going ramp period. Furthermore, when applying the second fast (1.8 > 1.2 V/μs) voltage slope ramp waveform, the corresponding IR emission remained almost the same as that of the conventional voltage slope ramp waveform, which meant that the IR emission was not intensified even at the fast voltage increase condition. This phenomenon is due to the presence of the priming particles produced prior to the application of the second fast voltage-slope ramp waveform. That is, the presence of the priming particles would contribute to suppressing a strong discharge even at a faster voltage slope ramp waveform and to alleviate the discharge instability due to the X-bias, thus resulting in the low background luminance stably during a short reset time. As shown in (III) of case 1 in Fig. 5(c), in the case of the slower (0.4 ≪ 1.2 V/μs) case, the IR emission was not found nearly during the first slow-

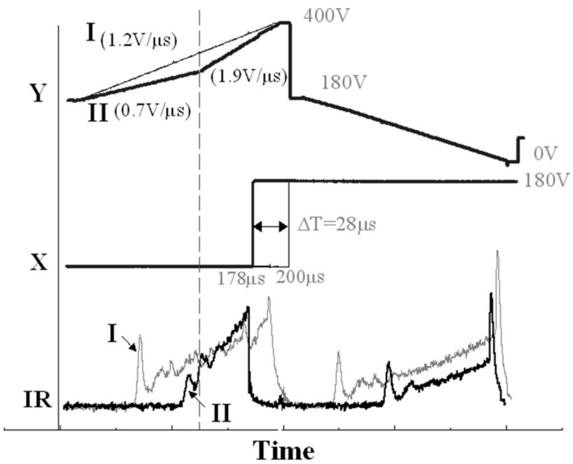

Fig. 6 Changes in IR emission waveforms when applying conventional and optimized DSR reset waveforms.

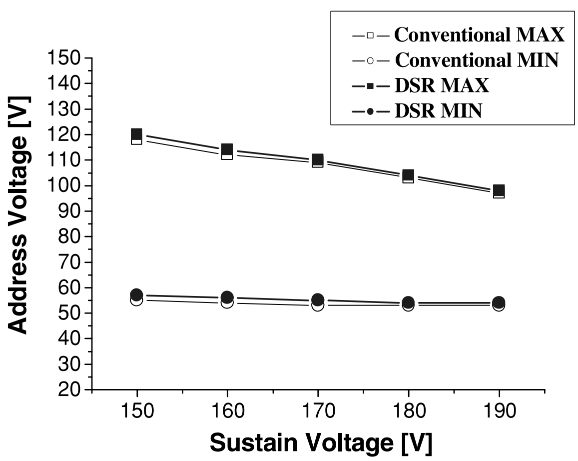

Fig. 7 Comparison of dynamic voltage margins when adopting conventional reset and optimized DSR reset waveforms.

voltage-slope ramp period, and the impulse-like IR emission peak was found during the second fast voltage-slope period. This experimental result indicates that the unstable reset discharge can be produced at the faster voltage slope condition especially for the case of no priming particles. As shown in Fig. 5(d), when ΔV_1 was increased, the background luminance was also increased, yet the minimum address voltage was decreased. However, as shown in Fig. 5(e), when the ΔT_2 was increased, the background luminance was decreased, but the minimum address voltage remained almost constant.

Finally, the changes in the IR waveforms and a comparison of the dynamic voltage margins are shown in Figs. 6 and 7, respectively, when applying the conventional and optimized DSR reset waveforms. The results in Figs. 6 and 7 confirm that the optimized reset waveform was able to reduce the background luminance within a stable dynamic margin, thereby enhancing the dark room contrast ratio. The detailed performances of the conventional and optimized DSR reset waveforms are compared in Table 2, where the

Table 2 Performance comparison between conventional and proposed DSR reset waveforms.

	Conventional Reset Waveform	Proposed DSR Reset Waveform	
Ramp voltage slope	Single slope	Dual slope	
Voltage slope during ramp-up period	1.2 V/μs	First slope	Second slope
		0.7 V/μs	1.9 V/μs
Vbias during ramp-up period	0 V	First slope	Second slope
		0 V	180 V
Voltage slope during ramp-down period	1.2 V/μs	1.2 V/μs	
Background luminance	1.58 cd/m^2	0.89 cd/m^2 (43%)	
Display luminance	278 cd/m^2	278 cd/m^2	
Dark room contrast ratio	175.94	312.35 (77%)	
Address minimum voltage	54 V	54 V	
Common conditions	10 reset periods (=10 sub field)/frame 7 inch test panel (42Bus) Vreset: 400 V Vscan: 70 V Vsustain: 180 V No selective reset		

background luminance with the proposed DSR reset waveform was reduced to 43 % of the background luminance generated by the conventional ramp reset waveform without reducing the minimum address voltage. Consequently, when adopting the DSR reset waveform, the dark room contrast ratio was improved by about 77%.

4. Conclusion

A new dual-slope ramp (DSR) reset waveform was proposed to improve the dark room contrast ratio in AC-PDPs. The proposed reset waveform has two different voltage slopes during a ramp-up period. The first voltage slope lower than the conventional ramp voltage slope plays a role in producing the priming particles under the low background luminance, thereby suppressing a strong discharge and alleviating a discharge instability even at the subsequent fast voltage-slope ramp waveform. Furthermore, the priming particles produced by the first slow voltage-slope ramp waveform can contribute to preventing the deterioration of the address discharge when applying the X-bias during a part of the second voltage-slope period to reduce further the background luminance. As a result, when adopting the optimized DSR reset waveform, the dark room contrast ratio was improved by about 77%. Consequently, the proposed DSR reset waveform can improve the dark room contrast and support a higher image quality for AC-PDPs.

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