Bipolar Scan Driving Scheme for High-Speed Address in AC PDP

Soo-Kwan Jang, Ki-Hyung Park, and Heung-Sik Tae

School of Electronic and Electrical Engineering, Kyungpook National University,
1370 Sankyuk-Dong, Buk-Gu, Daegu 702-701, Korea.
Phone: +82-53-950-6563, Fax: +82-53-950-5505, E-mail: hstae@ee.knu.ac.kr

ABSTRACT

This paper proposes a bipolar scan-driving scheme with a scan pulse width of 1μs for a high-speed address in ac-PDP. In order to produce the fast address discharge stably using the bipolar scan pulse during an address-period, the reset waveform is newly designed based on the V_t close curve analysis, and the address discharge characteristics are examined under various reset and scan waveforms.

INTRODUCTION

The fast address technique is the one of the most important issues of an ac-PDP for the realization of a high-class display device. The fast address can achieve an improvement of an image quality, luminance, contrast ratio, and peak luminance, and so on [1]. In general, it is difficult to produce the address discharge during a very short period, for example, 1μs because enough time is necessary for generating and accumulating the wall charges for the ensuing sustain discharge. In the previous paper, the authors have suggested that the bipolar scan waveform that can reduce the address time considerably. The bipolar scan waveform uses the two-step scan pulse with two polarities, which can separate the conventional address discharge into two different discharge modes: a space charge generation mode produced by the first step scan pulse with a negative polarity and a wall charge accumulation mode produced by the second step scan pulse with a positive polarity [2]. In the proposed scheme, since the second step scan pulse with a positive polarity produces another discharge between the X and Y electrodes so as to accumulate the wall charges, the negative bias is applied to the X electrode, unlike the conventional driving method that applies the positive bias to the X electrode. Accordingly, the conventional reset waveform is not applicable to the proposed bipolar scan driving method.

In this paper, the new reset waveform applicable to the bipolar scan-driving scheme is designed based on the V_t close curve analysis suggested by K. Sakita, *et al*. [3]. In order to investigate the address discharge characteristics produced by the bipolar scan pulse, the various voltage parameters, such as the set-down voltage, V_{SD}, the bias voltage, V_B for the reset waveform, and the negative bias voltage, V_Z, the reverse voltage, V_R, and address voltage, V_A for the bipolar scan waveforms, were varied under no misfiring condition guarantee -ed by the checkered pattern of 4-inch test panel.

OPERATION PRINCIPLE OF BIPOLAR SCAN WAVEFORM FOR HIGH-SPEED ADDRESS

Fig. 1 shows the proposed bipolar scan-driving scheme for a high-speed address in an ac-PDP. As shown in Fig. 1, the

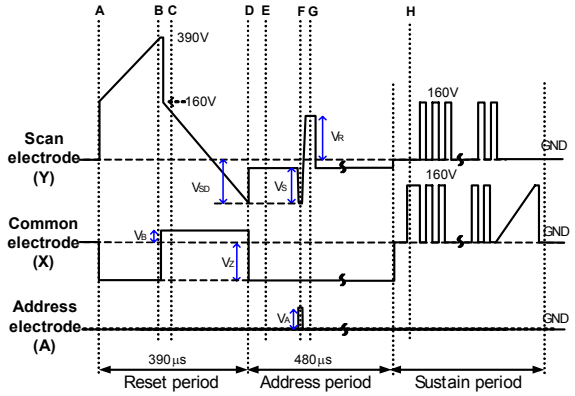

Fig. 1. Proposed bipolar scan driving scheme for fast address.

bipolar scan pulse with two polarities is applied to the Y electrode during an address-period. The first step pulse (< 0) in the bipolar scan waveform is a forward scan pulse with a negative polarity that is similar to the conventional scan pulse. Since its main function is to generate the wall charges with an application of the address pulse V_A during an address discharge, its width can be reduced within 1μs. Since the total address time is determined by the width of the forward scan pulse in the bipolar scan waveform, it is expected that the total address time can be reduced considerably. The second step pulse, V_R (>0) in the bipolar scan waveform is a reverse scan pulse with a positive polarity, and its main function is to accumulate the wall charges by producing another discharge between the Y and X electrodes immediately after the address discharge induced by the forward scan pulse. Thus, unlike the conventional case, the negative bias, V_Z (< 0) is applied to the X electrode, as shown in Fig. 1.

DESIGN OF RESET WAVEFORM BASED ON V_t CLOSE CURVE ANALYSIS

The reset waveform suitable for the bipolar scan waveform is designed and the V_t close curve is measured to analyze the proposed reset waveform from the 4-inch test panel. The V_t close curve is defined as a close curve formed by the cell voltage vector on the cell voltage plane, where a break down condition is satisfied [3]. The measured hexagonal-shaped V_t close curve shown in Fig. 2 provides information about the firing voltage condition among the three electrodes of the 4-inch test panel employed in this research: the firing voltage between the scan and address electrodes is 170V under the MgO cathode condition and 230V under the phosphor cathode condition. Fig. 2 shows the trajectories in the cell and wall voltages depending on the voltage level applied during the

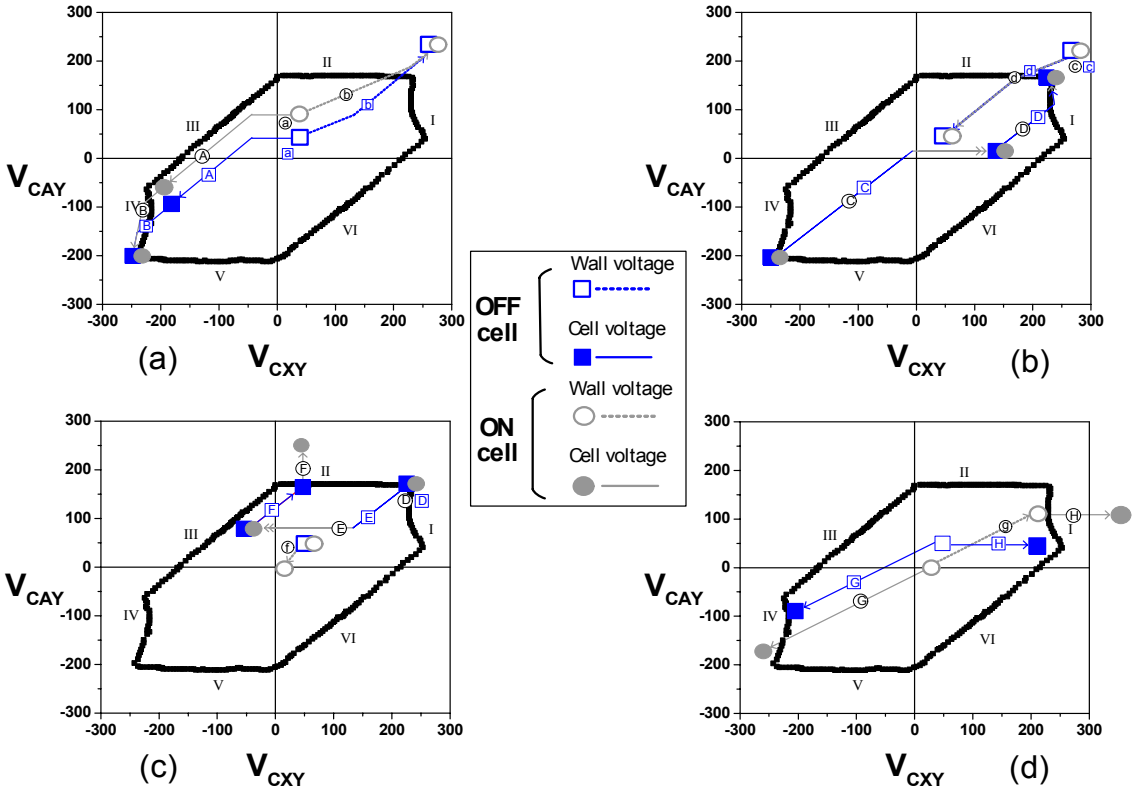

Fig. 2 Trajectories of cell voltage and wall voltage on cell voltage plane relative to applied voltages during reset- and address-periods: (a) set-up region, (b) set-down region, (c) wall charge generation region, and (d) wall charge accumulation region, Ⅰ: V_{tXY} (=Discharge start threshold cell voltage between X and Y), Ⅱ: V_{tAY} (=Discharge start threshold cell voltage between A and Y), Ⅲ: V_{tAX} (=Discharge start threshold cell voltage between A and X), Ⅳ: V_{tYX} (=Discharge start threshold cell voltage between Y and X), Ⅴ: V_{tYA} (=Discharge start threshold cell voltage between Y and A), and Ⅵ: V_{tXA} (=Discharge start threshold cell voltage between X and A).

reset- and address-periods on the cell voltage plane with the V_t close curve measured from the 4-in. test panel. The changes in the cell and wall voltages for both the on- and off-cells according to the driving waveform shown in Fig. 1 are described in the V_t close curve on the cell voltage plane as follows.

ⅰ) Ramp set-up region in reset-period (A-B in Fig. 1):

For both the on- and off-cells with initial wall charges, by applying +160V and $-V_Z$ (= -80V) to the Y and X electrodes (A point in Fig. 1.), respectively, the cell voltages move to the lower-left (a→A), but the wall voltages does not change because there is no discharge, as shown in Fig. 2 (a). As the ramp voltage applied to the Y electrode (hereinafter scan ramp voltage) increases slowly from +160 toward +390V and the voltage applied to the X electrode (hereinafter common voltage) remains at –80V, the cell voltage exceeds the one side (V_{tYX}: Ⅳ) of the V_t close curve, which means that the weak discharge is produced between the Y and X electrodes (Ⅳ: YX discharge region). During the ramp-up period, the negative bias voltage (= -80V) is applied to the X electrode so as to produce the surface discharge instead of the face discharge for the stable reset discharge by prohibiting the phosphor-cathode discharge condition. In the YX discharge region, the cell voltage reaches the simultaneous discharge point (=an intersection point between V_{tYX} and V_{tYA}) of the V_t close curve through the several weak discharges during ramp-up period. The scan ramp voltage increases until the cell voltages for both the on- and off-cells reach the simultaneous discharge point. In this case, the ramp set-up voltage is 390V. When the YX discharge occurs, the wall voltages moves to the polarity opposite to the applied voltage by the slope of 1/2. On the other hand, when the simultaneous discharges (YX and YA discharges) occur, the wall voltages move to the polarity opposite to the applied voltage by the slope of 1, as shown in the upper-right in Fig. 1 (a). As a result, the wall voltages move to the same point (a→b) irrespective of the on- or off-cell at the point B in Fig. 1.

ⅱ) Ramp set-down region in reset-period (C-D in Fig. 1):

When the ramp set-up voltage is abruptly reduced from 390 to 160 V, the cell voltages moves to the upper-right (B→C) but the wall voltages do not change because there is no discharge, as shown in Fig. 2 (b). After that, as the ramp set-down voltage decreases from 160V to $-V_{SD}$, the cell voltages exceed the V_{tXY} (Ⅰ), thereby resulting in a weak XY discharge. Thus, the cell voltages move to the simultaneous initialization point (=an intersection point between V_{tXY} and V_{tAY}) along the V_t close curve (C→D). In this case, the high set-down voltage level is necessary for moving the cell voltages to the simultaneous initialization point. On the other hand, the wall voltages move with a slope of 1/2 since the XY

discharge is produced. In addition, when the simultaneous discharge (XY and AY discharge) is produced, the wall voltages move with a slope of 1. At the termination of the ramp set-down for both the on- and off-cells, the cell voltages are located at the simultaneous initialization point, and the wall voltages are located at the same point as the initial wall charge, meaning that the successful initialization is carried out through the reset process. In this case, the values of V_B and V_{SD} affects the location of the wall voltages that determines the sustain margin. Moreover, note that the values of V_B and V_{SD} should be controlled properly in order not produce the misfiring discharge when the negative bias, V_Z is applied during an address-period.

iii) Wall charge generation region in address-period (E-F in Fig. 1):

At point E in Fig. 1 where the scan voltage abruptly increases by V_S and the common voltage abruptly decreases by $V_B + V_Z$, the cell voltages move from D to E point, and the wall voltages do not change because there is no discharge. For the on-cell, when the negative scan pulse, V_S and the positive address pulse, V_A are simultaneously applied, the primary address discharge is produced, indicating that the resulting cell voltage for the on-cell exceeds the V_{tAY} (Ⅱ) in the V_t close curve, as shown in Fig. 2 (c). On the other hand, for the off-cell, the cell voltage does not exceed the V_{tAY} (Ⅱ) in the V_t close curve, because no address pulse is applied, as shown in Fig. 2 (c). Since the main function of the primary address discharge in the proposed bipolar scheme with very short address pulse width (<1μs) is only to generate the wall charges, the wall charges on the scan and address electrodes disappear almost during an address discharge, so that the wall voltage for the on-cell moves to the lower-left, but the wall voltage for the off-cell does not move, as shown in Fig. 2 (c).

iv) Wall charge accumulation region in address-period (G-H region in Fig. 1):

As shown at point G in Fig. 1, when the reverse positive scan pulse, V_R is applied immediately after applying the negative scan pulse, the potential difference between $+V_R$ and $-V_Z$ can produce another address discharge, *i.e.*, secondary address discharge only for the on-cell thanks to the presence of priming particles generated by the previous primary address discharge. For the off-cell, the potential difference between $+V_R$ and $-V_Z$ cannot produce secondary address discharge due to the absence of priming particles. Since the main function of secondary address discharge is to accumulate the wall charges for the subsequent sustain discharge, the width of the reverse positive scan pulse is given for about 4 μs. This secondary address discharge can be considered as a kind of first sustain discharge produced between the Y and X electrodes during an address-period. For on-cell, the cell voltage exceed the V_{tYX} (Ⅳ) in the V_t close curve when applying the reverse positive scan pulse (G), thereby resulting in a strong YX discharge. On the other hand, for off-cell, the cell voltage does not exceed the V_{tYX} (Ⅳ) in the V_t close curve when applying the reverse positive scan pulse (G) because the wall charge state of the off-cell is different from that of the on-cell. As a result, prior to the sustain-period, the wall voltages for both the on- and off-cells are located at g points, respectively, as shown in Fig. 2 (d). In the sustain-period, when the sustain pulse is applied to the X electrode, the sustain discharge is produced only for the on-cell, as shown in Fig. 2 (d).

EXPERIMENTS AND RESULTS

The 4-in. test panel with a gas mixture of Ne+ Xe (4%) and a pressure of 400 Torr was employed in this research, and its structure and dimensions were the same as the conventional 42-in. wide VGA grade PDP with a cell pitch of 360μm. Fig. 1 shows the proposed bipolar scan-driving scheme employed in this research. The setup voltage of reset waveform applied to the Y electrode was 390V and the set-down voltage, V_{SD} (<0) was varied from -100 to -140V. The positive bias voltage, V_B (>0) was changed from 20 to 60V during the set-down period, whereas the negative bias voltage, V_Z (<0) of the X electrode was changed from -65V to -85V during the setup and address period, as shown in Fig.1. The amplitudes of the negative scan pulse, V_S (<0) and reverse positive scan pulse, V_R (>0) were –90 and 160V. The total times of the reset- and address-periods were given for 390μs and 480μs, respectively. The amplitude of the sustain pulse was 160V and the operating frequency was 100 kHz. Fig. 3 shows the checkered pattern that consists of the 5×5 squares to display the white and black images alternately. This checkered pattern was used to check a misfiring discharge between adjacent cells: *i.e.*, the white square was surrounded by the black square and vice versa. The following experimental conditions were chosen only in the case of no misfiring discharge guaranteed by the checkered pattern shown in Fig. 3. Fig. 4 shows the changes in the IR wave- forms measured during the address discharge relative to various voltage levels, such as set-down voltages, V_{SD} and V_B, in reset-period, V_Z, V_R, and V_A, in address-period. The first IR emissions were emitted during a primary address discharge, whereas the second IR emissions were emitted during a secondary address discharge. The measured IR emission data of Fig. 4 (a) indicates that both the primary and secondary address discharge intensities strongly depend on the set-down voltage in the reset-period. As the amplitude of V_{SD} increases, the primary address discharge was intensified and the resultant secondary address discharge was also intensified. As mentioned in (ii), in order to move the cell voltages to the simultaneous initialization point in the V_t

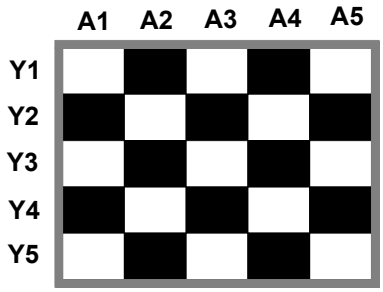

Fig. 3. Checkered pattern that consists of 5×5 squares employed to check misfiring discharge between adjacent cells.

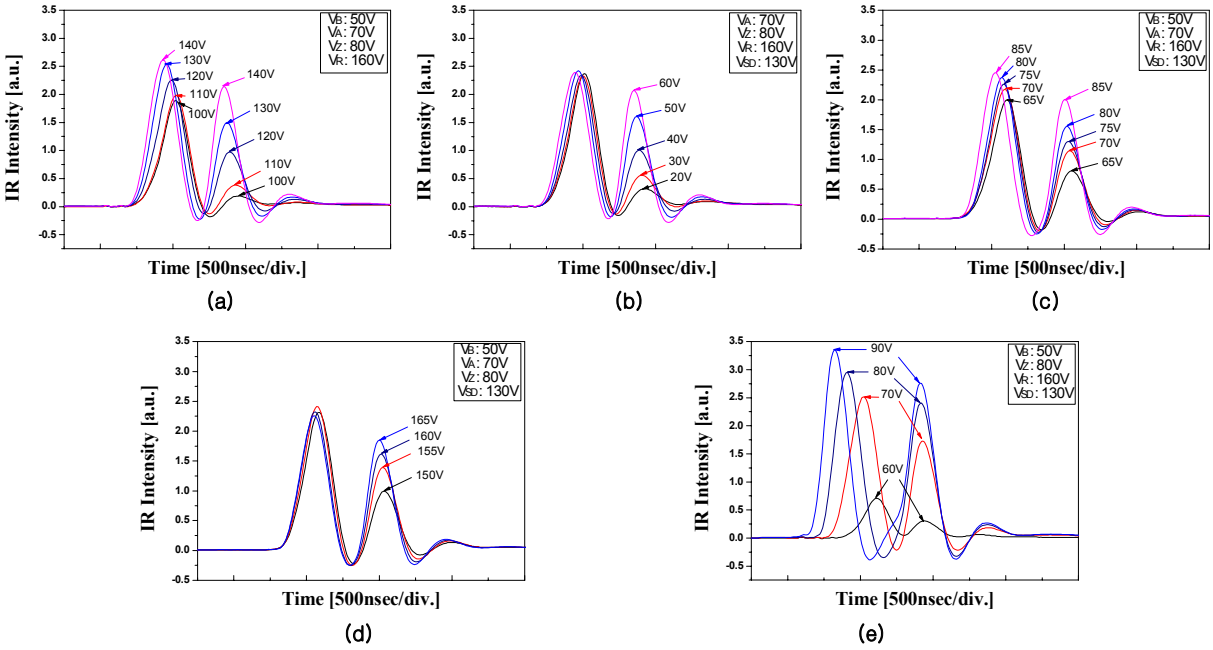

Fig. 4. IR waveforms measured during primary and secondary address discharges at various (a) set-down voltages, V_{SD}, (b) bias voltages, V_B, in reset-period, (c) negative bias voltages, V_Z, (d) reverse positive scan pulses, V_R, and (e) address pulse voltage, V_A, in address-period.

close curve, the application of the V_{SD} with a high voltage level is necessary in the reset-period. To facilitate the secondary address discharge, the minimization of the positive wall charges accumulated on the X electrode is necessary. In this sense, applying the positive bias, V_B to the X electrode enables the reset discharge to occur between X and Y electrodes instead of Y and A electrodes during the ramp set-down period, thus resulting in removing the more amount of the wall charges between X and Y electrodes. Accordingly, as the bias voltage, V_B increases, the secondary address discharge is intensified due to the decrease in the positive wall charges accumulated on the X electrode, as shown in Fig. 4 (b). However, too high bias voltage of 60V causes a misfiring discharge at E point in Fig. 1. As shown in Fig. 2 (c), too high value of V_B+V_Z causes the cell voltages to exceed the V_{tAX} (Ⅲ), thus resulting in a misfiring between A and Y electrodes. As a result, the bias voltage of 50V is adequate in this experiment. As shown in Fig. 4 (c), as the negative bias voltage, V_Z increases, the address discharge is intensified. However, too high V_Z of 85V may cause a misfiring. In this case, the negative bias voltage of 80V is proper. As shown in Fig. 4 (d), the secondary address discharge is intensified in proportion to the amplitude of the reverse positive scan pulse, V_R. As shown Fig. 4 (e), in proportion to the amplitude of address pulse, V_A, the primary address discharge intensity becomes stronger; thereby resulting in the larger amount of space charges. Thus, the ensuing secondary address discharge intensity became stronger. Fig.5 shows the dynamic margin measured using the checkered pattern in the case of adopting the proposed bipolar scan-driving scheme. As shown in Fig. 5, as a result of the optimization for the various voltage levels in the bipolar scan pulse, good dynamic margin characteristics are obtained.

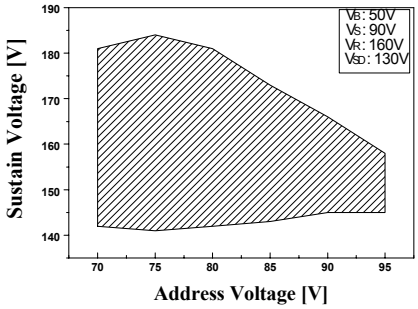

Fig. 5 Dynamic margin in case of adopting proposed bipolar scan driving scheme.

CONCLUSION

In this paper, a bipolar scan-driving scheme with a scan pulse width of 1μs is proposed for a high-speed address in an ac-PDP. Based on the V_t close curve analysis, the parameters such as V_{SD}, V_B, V_Z and V_R are chosen and its validity is tested under the checkered pattern. As result, the voltage levels of the bipolar scan waveform are determined within a stable operation range.

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