A Study on Wall-Charge Behavior of Single-Sustain Waveform Based on V_t Close-Curve Analysis in AC Plasma Display Panel

Byung-Gwon Cho and Heung-Sik Tae, *Senior Member, IEEE*

***Abstract*—The wall-charge behaviors of the conventional and two types of single-sustain waveforms during address and sustain periods are investigated based on a simulated result and a V_t close-curve analysis. The single-sustain waveform means that the sustain pulse having both positive and negative voltage levels is applied only to the single-side electrode, i.e., the scan (Y) electrode in this paper, where the common (X) electrode remains grounded. In the single-sustain waveform, the address discharge characteristics were observed to be improved by applying a higher voltage level without causing a misfiring discharge during an address period. An asymmetric IR emission was observed for both positive and negative sustain pulses during a sustain period, which was caused by the simultaneous discharge, including the plate gap discharge between the scan (Y) and the address (A) electrodes only when applying the negative sustain pulse to the scan (Y) electrode.**

***Index Terms*—Address discharge characteristics, asymmetric IR emission, plasma display panel (PDP), single-sustain waveform, V_t close-curve analysis, wall-charge behavior.**

I. Introduction

PLASMA display panel (PDP) has been considered to be the most promising candidate for digital television due to such conspicuous features as a slim-type large area ($>$ 40 in), a self-emitting-base good color reproduction capability, a wide dynamic contrast ratio, and a fast visible conversion response by the phosphor layer per sustain pulse [1], [2]. Thus, to capture the TV consumer market and maintain a lead over other flat-panel-display devices, the development of a low-cost driving technology for plasma TVs has become a critical issue. Most recent efforts have focused on reducing the address voltage [3], a single-scan method [4], and decreasing the number of electrical parts. The PDP was driven by applying the driving waveforms to the sustain (or common) (X), scan (Y), and address (A) electrodes [5]. In particular, the sustain waveform was alternately applied to the X and Y electrodes. If the two sustain pulses are merged to one sustain pulse with both the positive and negative voltage levels, that is to say, a sustain waveform is applied only to the Y electrode without applying any sustain driving waveform to the X electrode (hereinafter, this waveform is called the single-sustain waveform), the driving cost can be considerably reduced due to the elimination of the sustain driving-circuit block on the X electrodes. This type of driving waveform called an eliminated X-board (EX) driving waveform has already been reported [6]. However, the discharge characteristics and the wall-charge behaviors of the single-sustain waveforms were not discussed intensively.

In this paper, the wall-charge behaviors of the conventional and two types of single-sustain driving waveforms, including the EX driving waveform, are investigated, and the corresponding discharge characteristics, such as address and sustain discharges, are studied based on the simulated result and the V_t close-curve analysis [7], [8].

II. Single-Sustain Waveform

Fig. 1(a) and (b) shows the conventional sustain driving waveform applied alternately to the Y and X electrodes and the corresponding sustain driving circuit with energy recovery circuit, respectively [9]. Fig. 1(c) and (d) shows the proposed single-sustain driving waveform with positive and negative polarities applied only to the Y electrode and the corresponding driving circuit with energy recovery circuit [10]. As shown in Fig. 1(b) and (d), the conventional sustain waveform needs two times of switches for main sustain and energy recovery circuits compared with the switch number required for single-sustain driving circuit. On the other hand, the maximum voltage level for the single-sustain waveform requires a higher level than that for the conventional sustain waveform. Nonetheless, since the insulated gate bipolar transistors (IGBTs) instead of power metal–oxide–semiconductor field-effect transistors are used as switching devices in this experiment, the higher voltage level required for the single-sustain waveform causes just a little cost rise. Therefore, it is expected that for the single-sustain waveform, the circuit cost would be reduced because the reduced cost induced by eliminating the driving switches is higher than that induced by lowering the voltage level. That is, the conventional driving circuit in Fig. 1(b) needs eight IGBTs, whereas the single-sustain circuit in Fig. 1(d) needs just four IGBTs. Accordingly, the circuit cost would be reduced a half in switching devices when adopting the single-sustain circuit compared with the conventional driving circuit.

Fig. 2 shows the (a) conventional and two types of single-sustain waveforms: (b) the first single-sustain waveform (case 1) and (c) the second single-sustain waveform (case 2),

Manuscript received April 5, 2007; revised October 15, 2007. This work was supported in part by the Brain Korea 21 in 2007.

B.-G. Cho is with Department of Electrical and Computer Engineering, University of Illinois, Urbana, IL 61801 USA.

H.-S. Tae is with School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu 702-701, Korea (e-mail: hstae@ee.knu.ac.kr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TPS.2007.913927

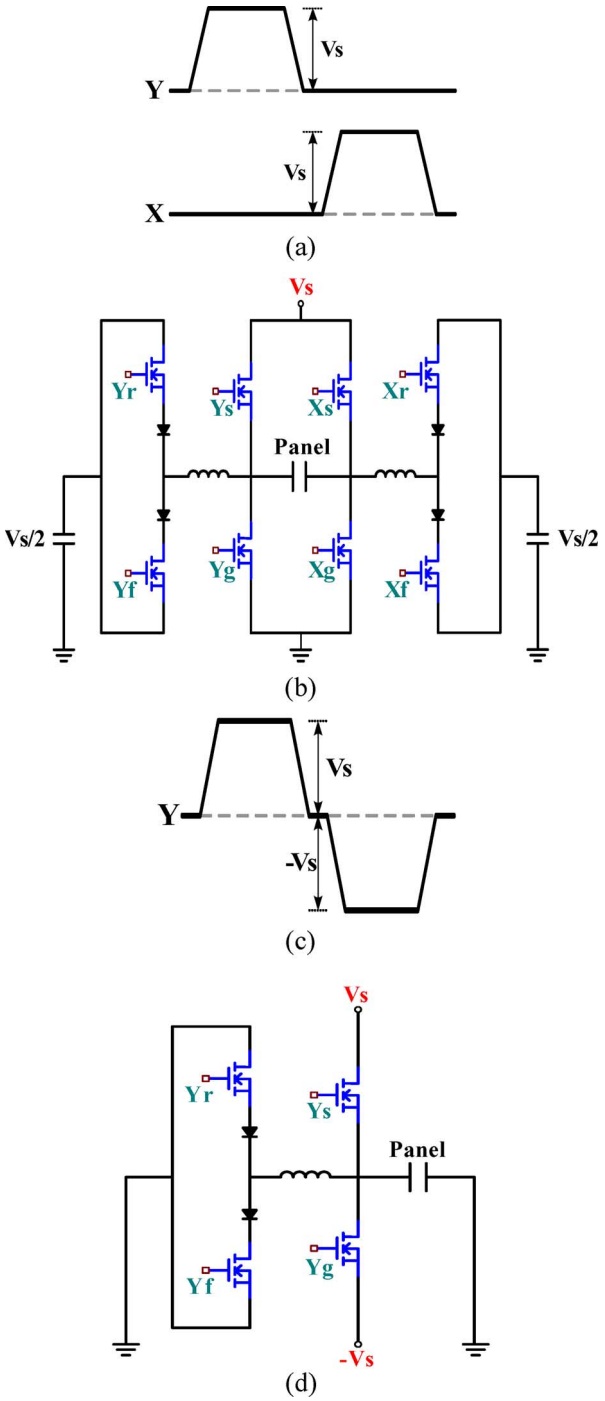

Fig. 1. (a) Conventional sustain pulses applied alternately to the Y and X electrodes. (b) Corresponding sustain driving circuit with energy recovery circuits. (c) Single-sustain driving waveform with the positive and negative polarities applied only to the Y electrode. (d) Corresponding sustain driving circuit with energy recovery circuits.

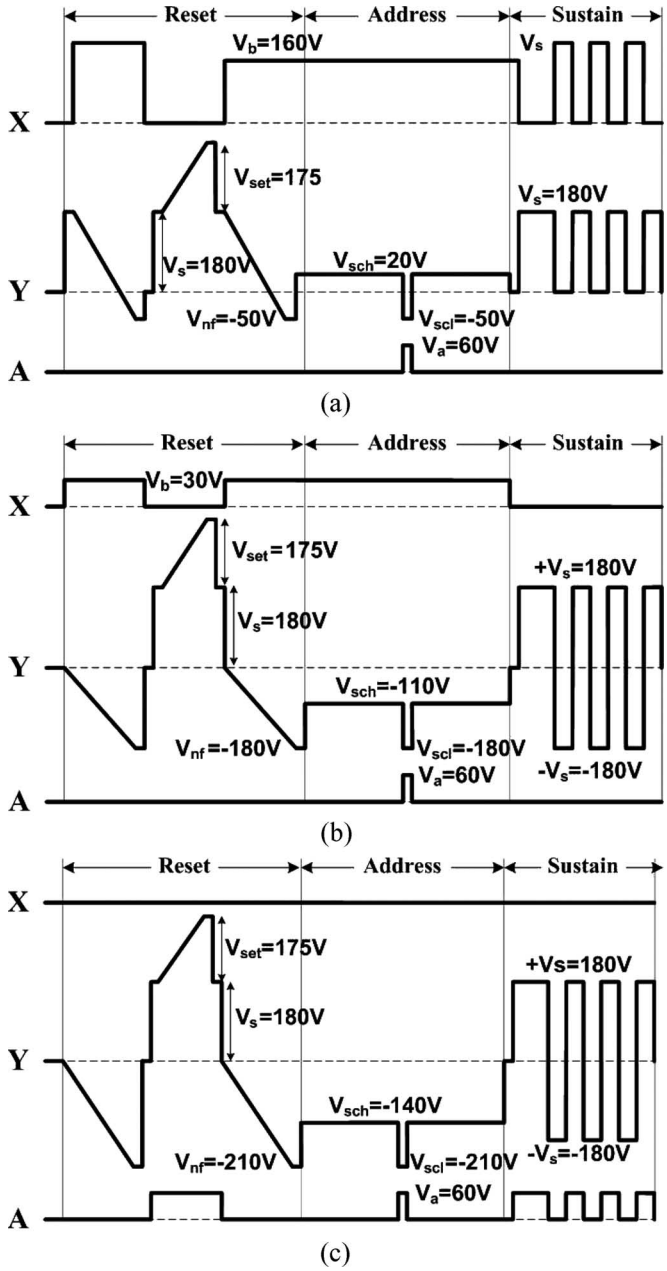

Fig. 2. (a) Conventional and two types of the single-sustain waveforms employed in this paper: (b) case 1 and (c) case 2.

including the reset, address, and sustain periods for the conventional 42-in panel structure with a Ne–Xe (7%) gas mixture. The common driving conditions were given as follows: a sustain voltage $(V_{\rm s})$ of 180 V, a reset voltage $(V_{\rm set})$ of 175 V, and an address voltage $(V_{\rm a})$ of 60 V. A scan-low voltage $(V_{\rm scl})$ and a bias voltage $(V_{\rm b})$ were -50 and 160 V, respectively, for the conventional driving waveform, whereas the scan-low voltages $(V_{\rm scl})$ were -180 V for case 1 and -210 V for case 2, and the bias voltages $(V_{\rm b})$ were 30 V for case 1 and 0 V for case 2. In the proposed driving waveforms in Fig. 2(b) and (c), the falling-ramp waveform was applied from the zero voltage level, and the scan-low voltage $(V_{\rm scl})$ during the address period was lower than that in the conventional driving waveform. In addition, the single-sustain waveform was applied only during a sustain period. In case 1, a small bias voltage was applied to erase the wall charges accumulated on the X electrode during an address period. However, because the falling-ramp voltage applied to the Y electrode in case 2 was lower than that in both the conventional and case 1, the wall charges between the Y–A electrodes were accumulated to the opposite polarity: That is, the ions were accumulated on the Y electrode, and the electrons were accumulated on the A electrode, when compared with the wall charges by the conventional method, which induced the

misfiring discharge during a sustain period. Accordingly, the address bias voltage during a sustain period in case 2 in Fig. 2(c) played a significant role to prevent the misfiring discharge [6].

III. Analysis of Three Driving Waveforms During Reset, Address, and Sustain Periods

A. Reset Waveforms

Fig. 3(a) shows the V_t close-curve on the applied voltage plane measured from the 42-in panel without initial wall charges before applying the driving waveforms shown in Fig. 2. The horizontal axis indicates the breakdown threshold voltage between the X–Y electrodes, whereas the vertical axis indicates the breakdown threshold voltage between the A–Y electrodes. The typical V_t close-curve shape in the conventional panel structure is a hexagon with six sides designating the breakdown threshold voltage. Thus, the inner region of the V_t close-curve in Fig. 3(a) means a nondischarge region, whereas the outer region means a discharge region [7], [8]. Fig. 3(b) shows three different V_t close-curves on the applied voltage plane measured after a reset period when applying the three different driving waveforms of Fig. 2(a)–(c), respectively. The result of the V_t close-curve analysis shown in Fig. 3(b) indicated that the wall charges between the X–Y electrodes were redistributed to the same amount irrespective of the types of driving waveforms, but the wall-charge distribution between the A–Y electrodes was changed considerably depending on the types of driving waveforms. As shown in Fig. 3(b), for the conventional case, the V_t close-curve was shifted to the lower direction with respect to the reference V_t close-curve of Fig. 3(a), which indicated that the ions were accumulated on the A electrode. The shape of the measured V_t close-curve in case 1 of Fig. 3(b) was almost similar to that in Fig. 3(a), which meant that for the first single-sustain waveform (case 1), the wall charges were almost erased on three electrodes. For the second single-sustain waveform (case 2), the V_t close-curve was shifted to the upper direction with respect to the reference V_t close-curve of Fig. 3(a), which showed that the wall charges with the opposite polarity, i.e., the electrons, were accumulated on the A electrode.

Fig. 3(c) shows the simultaneous initial points prior to the address discharge displayed on the applied voltage plane of the V_t close-curve for the conventional and the two types of single-sustain waveforms. The initial voltage points for the address discharge were different for three cases, and the A–Y gap voltages for three cases were close to the firing voltages by the scan-low voltage, respectively, as shown in Fig. 3(c). When the scan-low voltage was applied before applying the address pulse, the voltages were located at (210, 50) for the conventional case, (210, 180) for the first single-sustain case, and (210, 210) for the second single-sustain case on the V_t close-curves. For example, $(V_b - V_{scl}, 0 - V_{scl}) = (160 + 50, 0 + 50)$ for the conventional case, $(V_b - V_{scl}, 0 - V_{scl}) = (160 + 50, 0 + 180)$ for the first single-sustain case (case 1), and $(V_b - V_{scl}, 0 - V_{scl}) = (160 + 50, 0 + 210)$ for the second single-sustain case (case 2). Consequently, all A–Y gap voltages were initialized close to the firing voltage by the scan-low voltage for three cases, as shown in Fig. 3(c).

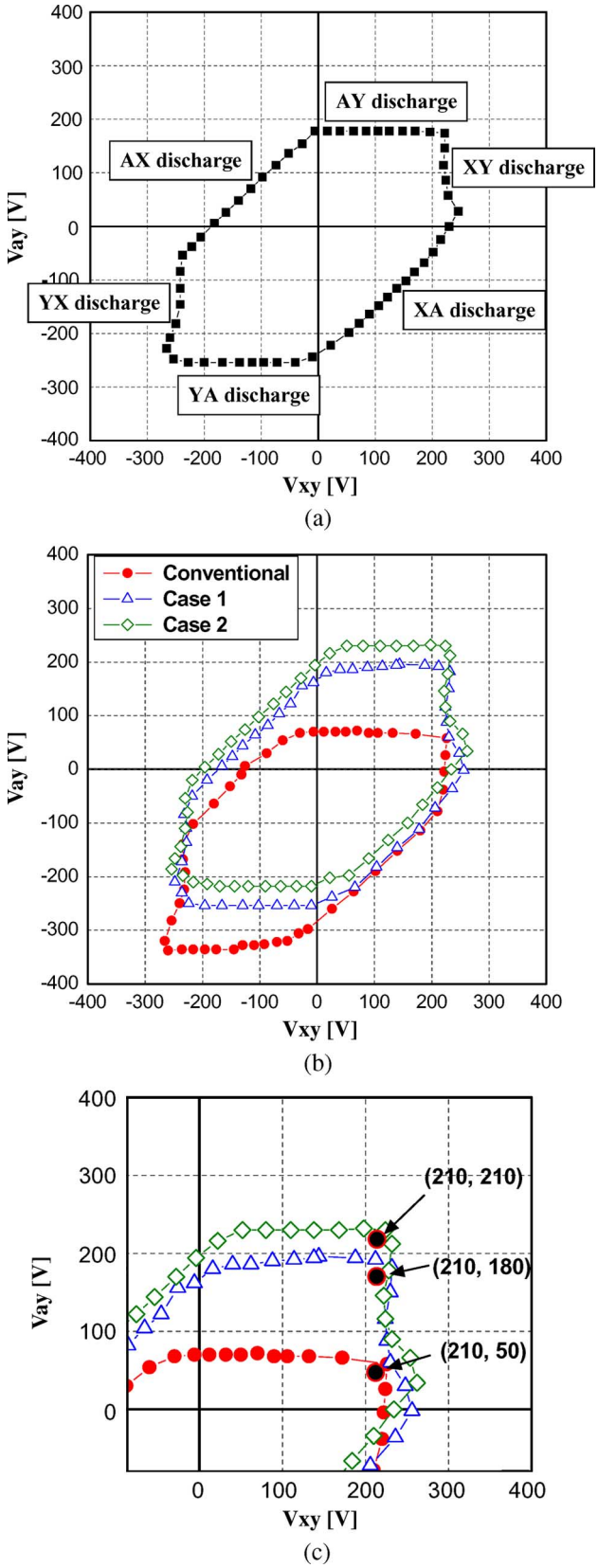

Fig. 3. (a) V_t close-curve measured on the applied voltage plane from a 42-in panel before applying the driving waveforms shown in Fig. 2. (b) V_t close-curves measured on the applied voltage plane after the reset period when applying three different types of driving waveforms, including the single-sustain waveforms shown in Fig. 2. (c) Simultaneous initial points prior to the address discharge displayed on the applied voltage plane of the V_t close-curve for the conventional and the two types of single-sustain waveforms.

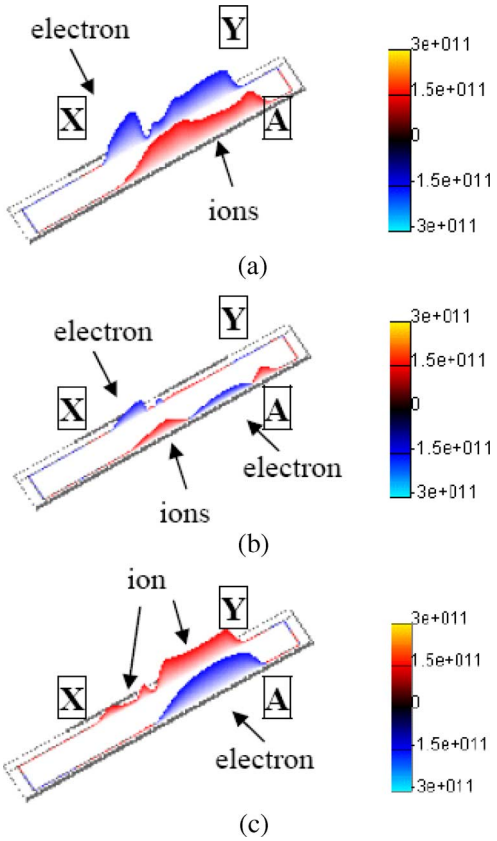

Fig. 4. Simulated results of the wall-charge distributions accumulating among the three electrodes after the reset period: (a) conventional, (b) case 1, and (c) case 2.

Fig. 4 shows the simulated results of the wall charges accumulating among the three electrodes after a reset period for three cases: (a) conventional, (b) first single-sustain (case 1), and (c) second single-sustain (case 2) waveforms. The simulator used in this experiment is based on the 2-D fluid model of plasma [11]. The simulated result of Fig. 4 validates the analysis result of the V_t close-curves in Fig. 3(b).

B. Address Discharge Characteristics

Fig. 5 shows the address discharge times measured after applying the scan pulse during an address period for three different types of driving waveforms in Fig. 2. As shown in Fig. 5(a), the address discharge time lags for the single-sustain waveforms were shorter than those for the conventional case. This result indicates that the first single-sustain waveform (case 1) shows the best address discharge probability, and the second single-sustain waveform (case 2) shows the better address discharge probability. For the conventional case, the address discharge strongly depends on the wall charges accumulated on the three electrodes prior to the address discharge. However, for cases 1 and 2, the address discharges strongly depend on the scan voltage level applied to the three electrodes during the address period because the wall charges accumulated on the three electrodes, particularly the X–Y electrodes, have been erased considerably prior to the address period. This wall-charge-erasing condition in cases 1 and 2 enables the application of

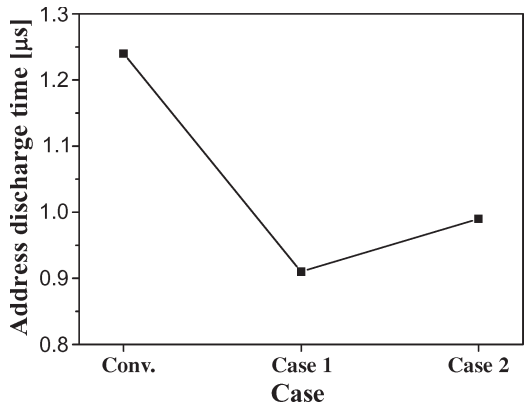

Fig. 5. Address discharge time lags measured after applying scan pulse during the address period for three different types of driving waveforms.

lower scan-low voltage ($V_{\rm scl}$) without a misfiring discharge for off-cells. Since the PDP has millions of microdischarge cells, the fast and stable address discharge using the wall charge accumulating on the three electrodes seems difficult to produce because of the nonuniform characteristics of the PDP. When comparing cases 1 and 2, the address discharge time lag in case 1 was slightly shorter than that in case 2 because the inversion phenomenon of the wall-charge polarity occurred in case 2.

To investigate which was the main factor for causing the shorter address discharge time lag phenomenon for the single-sustain waveforms, the discharge time lags were measured with respect to two factors, i.e., the variation in the wall charges prior to an address discharge and the variation in the address-voltage amplitude during an address period. In general, the falling-ramp voltage ($V_{\rm nf}$) in Fig. 2(a) is equal to the scan-low voltage ($V_{\rm scl}$). If the falling-ramp voltage is higher than the scan-low voltage ($\Delta V_{\rm y} = V_{\rm nf} - V_{\rm scl} > 0$) (in this case, the scan-low voltage ($|V_{\rm scl}|$) is fixed at a proper level), the reduction of wall charges is minimized, so that the subsequent address discharge time is shortened by the wall charges on the three electrodes. In this case, since the wall charges set up during the ramp-up period are less erased during the ramp-falling period, the improvement of the address characteristics is attributed mainly to the wall charges accumulating on the Y and A electrodes. On the other hand, if the amplitude of scan-low voltage is lower than that of the falling-ramp voltage (in this case, the falling ramp voltage is fixed at a proper level), $\Delta V_{\rm y}$ satisfies the line sequential priming addressing condition. Unlike the aforementioned case, the improvement of address discharge characteristics is caused mainly by the priming particles [7].

To compare which was a dominant factor to enhance the address discharge, the changes in the address discharge time lags were measured for three cases A, B, and C. As shown in Fig. 6(a), for case A, $V_{\rm scl}$ was fixed at -50 V, and $V_{\rm a}$ was fixed at 60 V. Only $V_{\rm nf}$ was varied from -50 to -30 V, where $\Delta V_{\rm y1} = 10$ V means that $V_{\rm nf} = -40$ V, and $\Delta V_{\rm y1} = 20$ V means that $V_{\rm nf} = -30$ V. For case B, $V_{\rm nf}$ was fixed at -50 V, and $V_{\rm a}$ was fixed at 60 V. Only $V_{\rm scl}$ was varied from -50 to -70 V, where $\Delta V_{\rm y2} = 10$ V means that $V_{\rm scl} = -60$ V, and $\Delta V_{\rm y2} = 20$ V means that $V_{\rm nf} = -70$ V. For case C, $V_{\rm nf}$ was fixed at -50 V, and $V_{\rm scl}$ was fixed at -50 V. Only $V_{\rm a}$ was varied from 60 to 80 V, where $\Delta V_{\rm a} = 10$ V means that $V_{\rm a} = 70$ V,

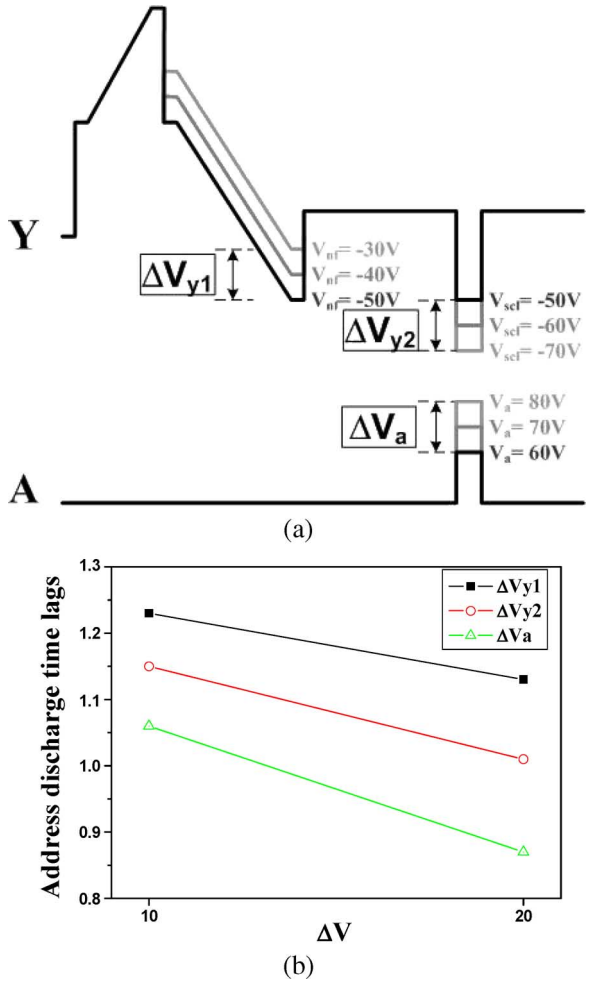

Fig. 6. (a) Variations in ΔV_{y1}, ΔV_{y2}, and ΔV_a in the conventional driving waveform of Fig. 2(a). (b) Corresponding address discharge time lags when ΔV_{y1}, ΔV_{y2}, and ΔV_a are varied by 10 and 20 V.

and $\Delta V_a = 20$ V means that $V_a = 80$ V. As shown in Fig. 6(b), when the address voltage was increased, the address discharge time was shown to be the best shortened. For two cases, ΔV_{y1} and ΔV_{y2}, the variation in ΔV_{y2} was shown to be more effective in reducing the address discharge time. This result illustrates that the application of the higher applied voltage during an address discharge (i.e., case C) instead of the use of the wall charges (i.e., cases A and B) is favorable in obtaining the better address discharge characteristics.

Fig. 7 shows the address-voltage margin for three cases: conventional case, first single-sustain waveform (case 1), and second single-sustain waveform (case 2). For three cases, the maximum address voltages were almost the same, but the low minimum address voltage was obtained under the single-sustain waveform condition. In particular, the minimum address voltage in the second single-sustain waveform was lower than that in the first single-sustain waveform because the address discharge was more intensive in the second single-sustain waveform, as shown in Fig. 5(c) and (d).

C. Address Discharge Characteristics

Fig. 8(a) shows the driving waveforms for the conventional and the single-sustain waveforms and the two measuring points

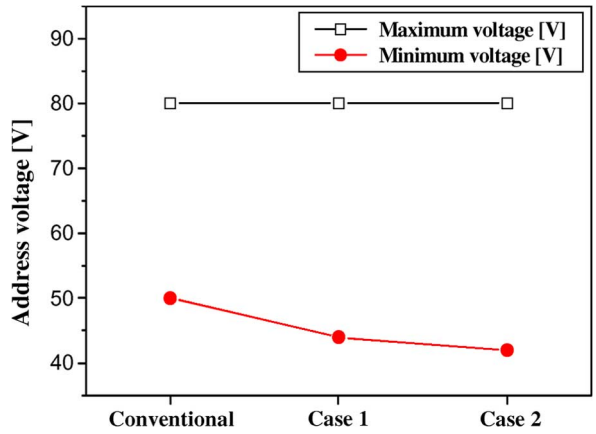

Fig. 7. Address-voltage margin for three cases: conventional case, first single-sustain waveform (case 1), and second single-sustain waveform (case 2).

of V_t close-curves: 1) after positive X-pulse for the conventional case and after negative Y-pulse for the single-sustain waveform; and 2) after positive Y-pulse for the conventional case and after positive Y-pulse for the single-sustain waveform. Fig. 8(b) shows the V_t close-curves measured at (I) of Fig. 8(a) for three cases, and Fig. 8(c) shows the wall-charge behavior diagram designated from the shift of the V_t close-curves with respect to the reference V_t close-curve with no initial wall charge in Fig. 8(b). As shown in Fig. 8(b), for the conventional case, the V_t close-curve after applying the positive X-sustain pulse was shifted to the right direction with respect to the reference V_t close-curve. From the shift of the V_t close-curve in Fig. 8(b), the resultant wall charges accumulated on the three electrodes were obtained as follows: the electrons on the X electrode and the ions on both the Y and A electrodes, as shown in Fig. 8(c)–(i). For the single-sustain cases, the V_t close-curve measured after applying the negative Y-sustain pulse to the Y electrode was shifted to the upper right direction with respect to the reference V_t close-curve. From the shift of the V_t close-curve in Fig. 8(b), the resultant wall charges accumulated on the three electrodes were obtained as follows: the electrons on the X and A electrodes and the ions on the Y electrodes, as shown in Fig. 8(c)–(ii) and (iii). The V_t close-curve analysis in Fig. 8(b) also provides information about the simultaneous discharge between the X–Y electrodes and between the A–Y electrodes. Since all the next sustain pulses had positive polarities for three cases, the next sustain voltage vectors $+V_s$ (Y) were moved to the third quadrant on the applied voltage plane, as shown in Fig. 8(b). In the conventional case, the next sustain voltage vector exceeded only the YX discharge region, which meant that the sustain discharge was produced only between the Y–X electrodes. On the other hand, in the single-sustain waveforms, the next voltage vectors exceeded the simultaneous discharge region between the YX and the YA discharge regions. In particular, for case 2, the simultaneous application of address pulse during the application of the next positive sustain pulse could change the voltage vector direction, which resulted in exceeding the YX discharge region, as shown in Fig. 8(b). Fig. 8(d) shows the V_t close-curves measured at (II) of Fig. 8(a) for three cases, and Fig. 8(e) shows the

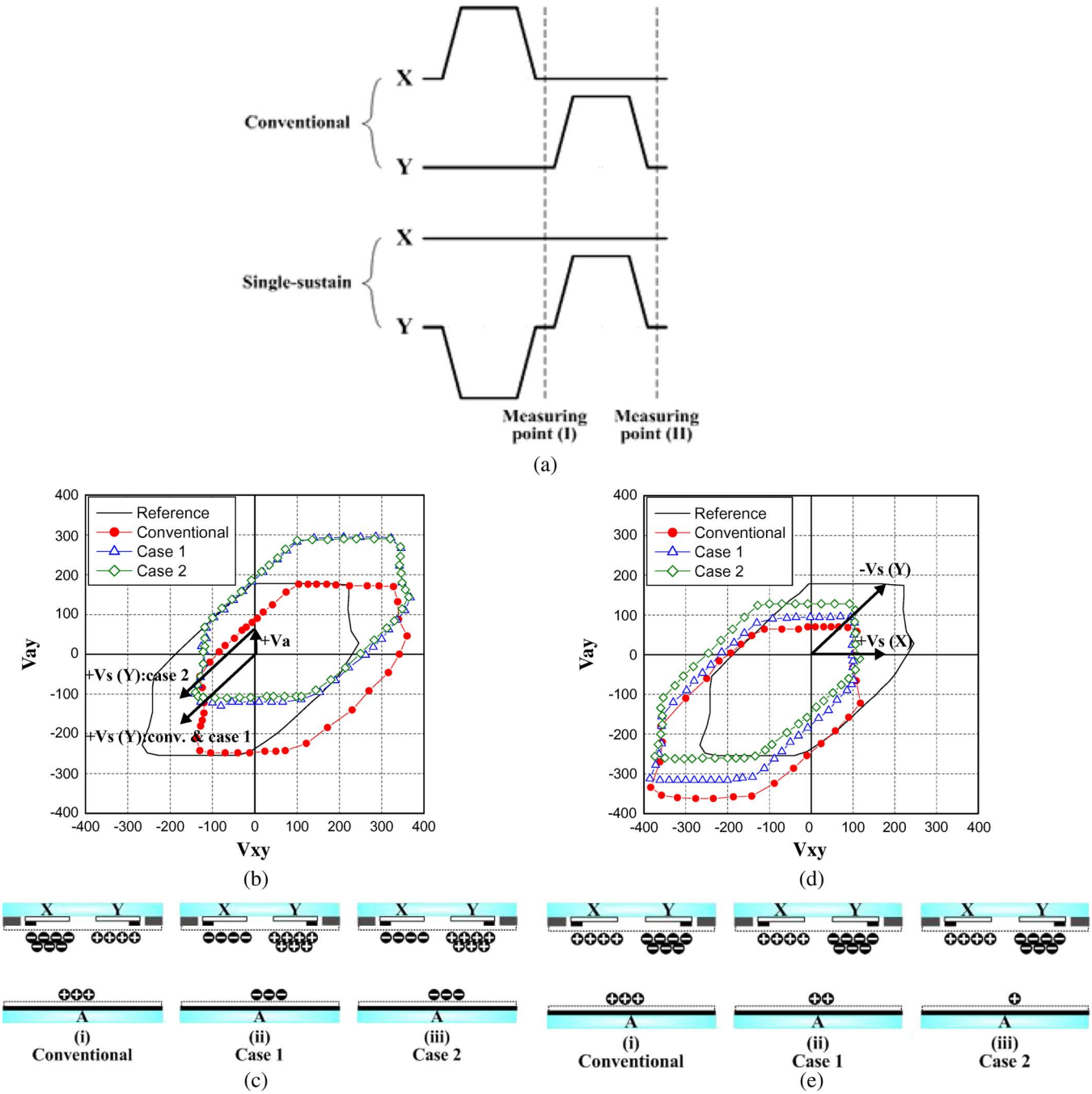

Fig. 8. (a) Sustain driving waveforms for the conventional and the single-sustain waveforms and the two measuring points of V_t close-curves: (I) and (II). (b) V_t close-curves measured at (I) in (a) on the applied voltage plane after the positive X-pulse for the conventional case and after the negative pulses in the single-sustain cases. (c) Wall-charge behavior diagram designated from the shift of V_t close-curves in (b). (d) V_t close-curves measured at (II) in (a) on the applied voltage plane after the positive Y-pulse for the conventional case and after the positive pulses for the single-sustain cases. (e) Wall-charge behavior diagram designated from the shift of the V_t close-curves in (d).

wall-charge behavior diagram designated from the shift of the V_t close-curves with respect to the reference V_t close-curve with no initial wall charge in Fig. 8(d). For the conventional case, the V_t close-curve in Fig. 8(d) was shifted to the lower left direction after applying the positive Y-sustain pulse, with respect to the reference V_t close-curve. The resultant wall charges were accumulated on the three electrodes as follows: the electrons on the Y electrode and the ions on both the X and A electrodes, as shown in Fig. 8(e)–(i). For the single-sustain case, the V_t close-curves after applying the positive Y-sustain pulse were less shifted to the lower left direction than that in the conventional case. The resultant wall charges were also accumulated on the three electrodes as follows: the electrons on the Y electrode and the ions on both the X and A electrodes, as shown in Fig. 8(e)–(ii) and (iii). For the three cases, the polarities of wall charges accumulating on the three electrodes were the same, as shown in Fig. 8(e)–(i), (ii) and (iii). However, the amount of wall charges accumulating on the A–Y

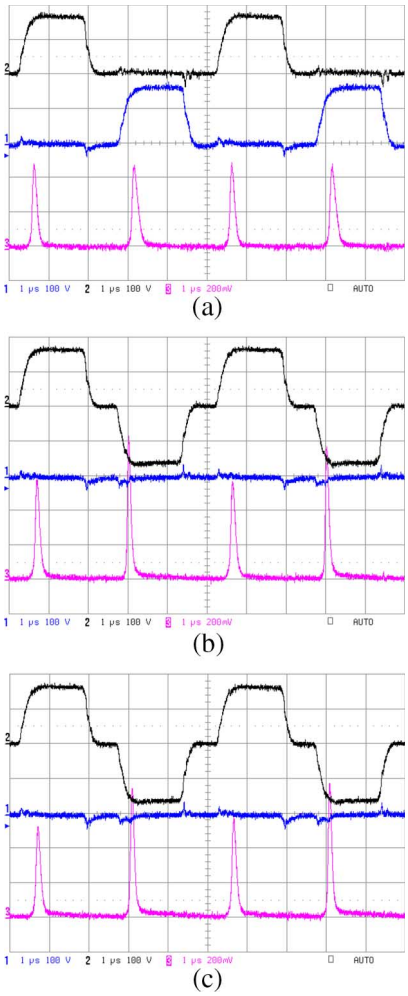

Fig. 9. Two sustain and corresponding IR (828 nm) waveforms during the sustain period among the three electrodes when applying (a) the conventional driving waveform and the single-sustain waveform of (b) case 1 and (c) case 2.

electrodes was quite different, even though the amount of wall charges accumulating between the X–Y electrodes was almost the same. In particular, as shown in Fig. 8(d), the V_t close-curve in case 2 was more shifted to the upper direction than that in case 1 because the accumulation of ions on the A electrode was suppressed due to the simultaneous application of the positive address pulse in case 2. For the single-sustain waveforms, since the next sustain pulses had negative polarities, the next sustain voltage vectors $-V_s$ (Y) were moved to the first quadrant on the applied voltage plane, thus exceeding the simultaneous discharge region between the XY and the AY discharge regions, as shown in Fig. 8(d).

Fig. 9 shows the two sustain and corresponding IR (828 nm) waveforms during a sustain period among the three electrodes when applying (a) the conventional driving waveform and the single-sustain waveform of (b) case 1 and (c) case 2. In comparing the IR emission waveforms for the single-sustain waveform in Fig. 9(b) and (c) with that for the conventional sustain pulse in Fig. 9(a), the stronger sustain discharge was produced in Fig. 9(b) and (c) because of the simultaneous discharge (X–Y and A–Y discharges), as shown in Fig. 8(b) and (d). In addition, for the single-sustain case, the negative sustain

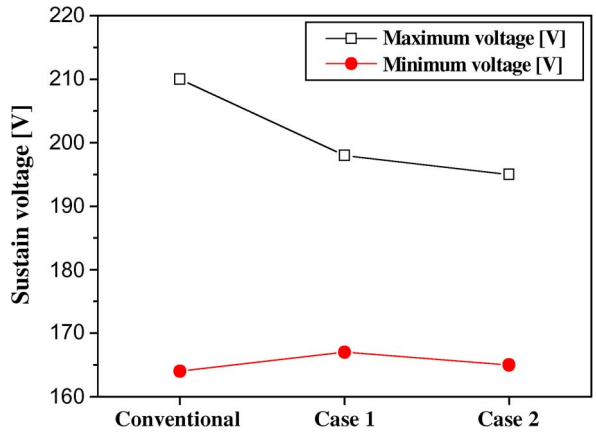

Fig. 10. Sustain-voltage margin for three cases: conventional case, first single-sustain waveform (case 1), and second single-sustain waveform (case 2).

pulse was observed to produce the stronger sustain discharge than the positive sustain pulse, as shown in Fig. 9(b) and (c). It appeared that this phenomenon was caused by the change of the MgO cathode condition between the Y–A electrodes in a cell when applying the negative sustain waveform. That is, unlike the positive sustain pulse, the ions were additionally bombarded toward the MgO layer with a higher secondary electron emission coefficient from the phosphor layer during the discharge produced by the negative sustain waveform, thereby resulting in an additional excitation or ionization [12].

Fig. 10 shows the sustain-voltage margin for three cases: the conventional case, the first single-sustain waveform (case 1), and the second single-sustain waveform (case 2). For the three cases, the minimum sustain voltage was similar within 5 V, but the maximum sustain voltages were low for the single-sustain waveforms. The low maximum sustain voltage for the single-sustain waveforms was due to the high discharge intensity during the negative sustain pulse-induced sustain discharge, as shown in Fig. 9.

IV. Conclusion

The wall-charge behaviors of the three cases, i.e., the conventional and the two types of single-sustain waveforms, are investigated based on the simulated result and the V_t close-curve analysis. For the single-sustain waveform, the address discharge characteristics were improved, which was caused by the effect of the higher external applied voltage during the address period than the accumulated wall charges during the reset period. In addition, an asymmetric intensive IR intensity during a sustain period was observed, which was caused by the simultaneous discharge, including the plate gap discharge between the Y–A electrode when applying the negative sustain pulse to the Y electrode.

References

[1] L. F. Weber, "The promise of plasma displays for HDTV," in *Proc. SID Dig.*, 2000, pp. 402–405.
[2] M. Uchidoi, "Fourth-generation PDPs: High image quality and low power consumption," in *Proc. SID Dig.*, 2004, pp. 202–205.

[3] Y. Takeda, M. Ishii, T. Shiga, and S. Mikoshiba, "A technique for reducing data pulse voltage in AC-PDP's using metastable-particle priming," in *Proc. IDW Dig.*, 1999, pp. 747–750.
[4] J.-Y. Yoo, B.-K. Min, D.-J. Myoung, K. Lim, E.-H. You, and M.-H. Park, "High speed-addressing method for single-scan of AC PDP," in *Proc. SID Dig.*, 2001, pp. 798–801.
[5] S. Kanagu, Y. Kanazawa, T. Shinoda, K. Yoshikawa, and T. Nanto, "A 31-in.-diagonal full-color surface-discharge AC plasma display panel," in *Proc. SID Dig.*, 1992, pp. 713–716.
[6] B.-G. Cho, H.-S. Tae, K. Ito, N.-S. Jung, and K.-S. Lee, "Study on discharge stability of cost-effective driving method based on $V_{\rm t}$ close-curve analysis in AC plasma-display panel," *IEEE Trans. Electron Devices*, vol. 53, no. 5, pp. 1112–1119, May 2006.
[7] K. Sakita, K. Takayama, K. Awamoto, and Y. Hashimoto, "High-speed address driving waveform analysis using wall voltage transfer function for three terminals and $V_{\rm t}$ close-curve in three-electrode surface-discharge AC-PDPs," in *Proc. SID Dig.*, 2001, pp. 1022–1025.
[8] H. Kim, J. Jeong, K. Kang, J. Seo, I. Son, K. Whang, and C. Park, "Voltage domain analysis and wall voltage measurement for surface-discharge type AC-PDP," in *Proc. SID Dig.*, 2001, pp. 1026–1029.
[9] L. F. Weber and M. B. Wood, "Energy recovery sustain circuit for the AC plasma display," in *Proc. SID Dig.*, 1987, pp. 92–95.
[10] K. Ito, B.-G. Cho, M. K. Lee, J. W. Song, S.-C. Kim, H.-S. Tae, N.-S. Jung, and K.-S. Lee, "New two stage recovery driving method for low cost AC plasma display panel," in *Proc. IDW Dig.*, 2005, pp. 461–464.
[11] S.-B. Song, P.-Y. Park, H.-Y. Lee, J.-H. Seo, and D. Kang, "Stability of weak discharge at Y-reset period in plasma display panel discharge," *Surf. Coat. Technol.*, vol. 171, no. 1–3, pp. 140–143, Jul. 2002.
[12] J. K. Lim, C.-S. Park, B.-T. Choi, H.-S. Tae, and S.-I. Chien, "Improvement of luminance and luminous efficiency using new negative sustain waveform in AC-plasma display panel," in *Proc. SID Dig.*, 2006, pp. 597–600.

Byung-Gwon Cho received the B.S. and M.S. degrees in electronic and electrical engineering and the Ph.D. degree in the subject matter of new cost-effective driving method from Kyungpook National University, Daegu, Korea, in 2001, 2003, and 2006, respectively.

He was a Postdoctoral Researcher with the Kyungpook National University and contributed to the development of the ultrahigh-speed address driving scheme in 2007. He is currently with the Department of Electrical and Computer Engineering, University of Illinois, Urbana, IL, USA. His current research interests include plasma physics and driving-circuit design of plasma display panels.

Dr. Cho received the Outstanding Poster Paper Award in 2003 from The Korean Physical Symposium and the Outstanding Basic Research Technology Paper Award in 2005 from The Fifth International Meeting on Information Display.

Heung-Sik Tae (M'00–SM'05) received the B.S., M.S., and Ph.D. degrees in electrical engineering from Seoul National University, Seoul, Korea, in 1986, 1988, and 1994, respectively.

Since 1995, he has been a Professor with the School of Electrical Engineering and Computer Science, Kyungpook National University, Daegu, Korea. His research interests include the optical characterization and driving circuit of plasma display panels, the design of millimeter-wave guiding structure, and the electromagnetic wave propagation using metamaterial.

Dr. Tae is a member of the Society for Information Display. He has been serving as an Editor for the IEEE TRANSACTIONS ON ELECTRON DEVICES section on flat panel display since 2005.